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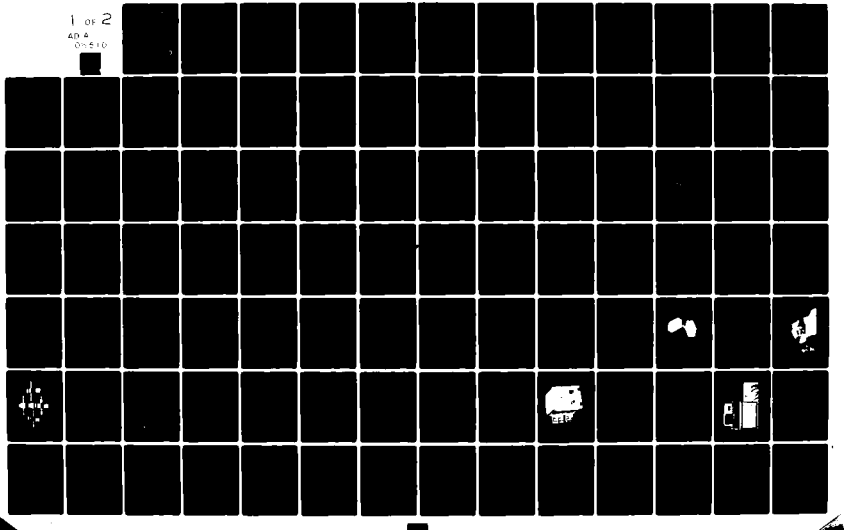

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ADVANCED CRASH SURVIVABLE FLIGHT DATA RECORDER AND ACCIDENT INFORMATION RETRIEVAL SYSTEM (AIRS)

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August 1981

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Prepared for
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Fort Eustis, Va. 23604

APPLIED TECHNOLOGY LABORATORY POSITION STATEMENT

This report describes a reasonable design approach to a helicopter Accident Information Retrieval System (AIRS) that records both flight and crash impact data which will aid accident investigations, reduce accidents, provide a sound basis for crashworthiness design criteria formulation, and could aid maintenance diagnostics and condition monitoring. The AIRS concept, detail designed and component and flight tested under this contractual effort, is characterized by low weight, small volume, low cost, and high reliability and has been proven to be technically feasible. The AIRS concept defined herein represents a quantum step towards the attainment of a compact low cost flight and crash impact data recorder that has application practicality for US Army helicopters. As a result of this program, the AIRS is advanced to the point where engineering development could be initiated. Additional Army programs relative to the AIRS will depend upon user support for ultimate aircraft application.

LeRoy T. Burrows of the Aeronautical Systems Division served as project engineer for this effort.

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The AIRS development program consisted of four phases.

Phase I: Detail Design Task:

Design concepts were formulated based on selection and definition of aircraft parameters to be monitored by the AIRS, selection of memory technology, circuit definitions for aircraft interfacing, and studies and tests

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related to the development of an armored module to protect the memory device.

The detailed design utilized signal conditioning for analog, synchro and discrete parameters, an Intel 8085 microprocessor, 32 kilobits of solid-state nonvolatile electrically alterable read only memory (EAROM), data compression and self test.

Phase II: Component Fabrication and Test

Using the concepts and design formulated in Phase I, Hamilton Standard fabricated and laboratory tested brassboard electronics units and developed and tested software which proved the feasibility of data collection and storage in a solid-state memory device utilizing unique data compression techniques to reproduce critical aircraft flight information. Flight-worthiness assurance tests were performed on the AIRS brassboard to assure operation in the flight test environment.

The concept developed to protect the memory storage device during and throughout an aircraft crash environment proved successful, as evidenced by the successful completion of the survivability tests on two prototype Crash Survivable Memory Modules (CSMM's).

Phase III: Brassboard AIRS Unit Flight Test Demonstration

The hardware fabricated and tested in Phase II was installed in a Sikorsky UH-60A BLACK HAWK helicopter S/N 77-22714. This aircraft is the first production aircraft of the series and is fully instrumented by Sikorsky for the purpose of flight test. Following verification of system installation and a safety of flight review, several test flights were accomplished and the data analyzed. Some developmental changes were incorporated in the AIRS during and as a result of the flight test program.

The flight test program demonstrated data compression capability ranging from 10:1 to 40:1 on the BLACK HAWK helicopter using a fixed frame, fixed interval, and variable frame technique. With 32 kilobits of memory and recording 19 continuous and 9 discrete parameters, a minimum of 15 minutes of data could be preserved in the event of an accident. Twenty minutes to an hour would be more normal.

Phase IV: Design Assessment

As a conclusion, the system was reviewed for final configuration, risk areas, final size and weight and life cost. Current estimates of a productionized AIRS electronics unit are weight, less than 9.3 pounds; volume, 207 cubic inches or less; and a mature reliability greater than 10,000 hours MTBF.

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INTRODUCTION

This report presents the results of engineering studies, design, hardware development, testing, and assessment of the Accident Information Retrieval System (AIRS).

The research conducted included evaluation of industry available memory devices leading to the joint selection by Hamilton Standard and the Army of a solid-state memory device suitable for application in the rigorous environment of a combat operational rotary-wing aircraft.

The development process continued with the implementation of the conceptual design reported in Reference 1. The hardware design was based on the latest state-of-the-art technology. Parameter studies were accomplished and software algorithms implemented, including unique data compression techniques developed by Hamilton Standard. These techniques allow the recording of aircraft data in relatively low digital data volume while preserving its integrity.

The resulting AIRS brassboard hardware successfully completed functional and flightworthiness tests to verify unit operational capabilities in the aircraft environment.

Flight testing of the AIRS was conducted on the Sikorsky BLACK HAWK (UH-60A) helicopter #77-22714 at Sikorsky's Flight Test and Development Center in West Palm Beach, Florida.

The heart of the AIRS is the Crash Survivable Memory Module (CSMM), which provides thermal and mechanical protection of the solid-state memory storage device. A CSMM that will protect the AIRS stored data through the severe crash environments of aircraft accidents was developed. The CSMM production prototype successfully withstood the rigorous survivability tests of the FAA test specification of Reference 2.

Following flight testing and data analysis, a design assessment was accomplished. This evaluation took into account test results, new information, and new technology components available. The resulting recommendations for refinements of the AIRS are included in this report.

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1. H. Ask, et al, PRELIMINARY DESIGN OF AN ACCIDENT INFORMATION RETRIEVAL SYSTEM (AIRS), USARTL 77-51, Applied Technology Laboratory, US Army Research and Technology Laboratories (AVRADCOM), Fort Eustis, Virginia, April 1978, AD055590.

2. U.S. Federal Aviation Regulation, Part 37.150, AIRCRAFT FLIGHT RECORDER TECHNICAL STANDING ORDER, TSO-C51a.

AIRS DESIGN GOALS AND GUIDELINES

The preliminary design report for AIRS [1] presented a recommended flight data recorder design concept. In this effort, the concept defined was developed into a detailed system, electrical, software, and mechanical design. This section details this design effort.

INPUT PARAMETER GUIDELINES

The basic function of the AIRS is to sense and store a set of data parameters which will supplement the investigation in determining the cause of an aircraft mishap. Data is also desired which will help determine the survivability of the impact as it relates to structures and ultimately the crew and passengers. (The basic AIRS design incorporates the potential of (with minor software design modifications) providing maintenance diagnostics and engine condition monitoring capabilities which would allow ground crew maintenance personnel to identify certain conditions of aircraft structure and/or engine overstress.) It is not practical or possible to gather all information that might be needed to assure that the cause of mishaps can be determined. Some parameters that might be desirable would be too expensive to obtain. Too many parameters would unnecessarily increase system cost and size or shorten recording time. The primary objective of the analysis was to determine the parameter list that gives the best compromise between necessary and desired recording capability and total cost and weight. Some parameter characteristics considered in order to determine the most effective total system design were:

1) The relative priority of the parameter (its technical value).

2) The incremental cost and weight of the parameter to include the effect on recording capacity and sensor requirements.

3) The desired accuracy.

4) The amount of change in the parameter that is significant enough to be noted.

Characteristic 2) above is airframe dependent in that in some airframes the signal is already available and in others a sensor must be added.

If the incremental value of a parameter was judged to be less than the incremental cost, that parameter was eliminated. Conversely, if the value was greater than the cost, then the parameter was included. Each parameter was considered individually on its own value versus cost. This resulted in some higher priority parameters being discarded while some lower priority parameters were retained. By this process, a cost effective system capability was estimated.

The desired accuracy, resolution, and threshold of significant change of a parameter determine the requirements for the electronic interface, data processing, and the memory size. For example, for a digital system the required accuracy determines the size of the analog to digital converter and the data word size. The recording threshold value and resolution determine the amount of data compression that is possible. The degree of compression determines the amount of data that can be stored in a given memory in a given time period.

The candidate parameter lists for the UH-60A shown in Tables 1, 2, and 3 and for the AAH in Table 4 were assembled using parameters found to be prevalent in the industry. These parameters have been reviewed with personnel from the US Army Agency for Aviation Safety and other agencies at Fort Rucker involved in accident investigation and represent the final list of parameters selected for inclusion in the production AIRS design.

Other parameters considered included radar altitude and throttle position. Radar altitude would be usable if readily available. Throttle might be valuable to distinguish power changes that were crew initiated from those due to engine problems.

AIRS DESIGN REQUIREMENTS AND GOALS

The following subsections describe the AIRS requirements as set forth by the Army along with an update on the recommended AIRS concept defined in Reference 1. The AIRS production system has the following requirements and design goals.

Required Features

(1) Record Flight and Crash Impact Data

The recording of crash impact data adds a new dimension to flight recorders of the past. Indeed, flight recorders of the past by virtue of their electromechanical implementation only had the capability for recording data prior to the time of an incident. Solid-state design will allow a very high tolerance in basic AIRS construction to allow the measurement of impact forces in the vast majority of helicopter mishaps.

(2) Design Life Greater Than 5000 Hours

The completely solid-state approach to the AIRS unit will allow attainment of a high degree of reliability. The only areas requiring extra emphasis with regard to this requirement are sensors. Here it is a matter of sensor cost versus life, as was described in the Reference 1 report. Potentiometric type devices, under certain circumstances, will exhibit life limits approximating the desired design life.

TABLE 1. BLACK HAWK (UH-60A) PARAMETER LIST (DC ANALOGS)

PARAMETER	DATA RANGE	SIGNAL RANGE (IN VDC)	RESOLUTION	LIMIT EXCEEDANCE
Airspeed	30 to 180k	2.25 to 13.5	3.04k	6.08k
Engine #1 Torque	0 to 150%	0 to 5.277	2.23%	4.46%
Engine #2 Torque	0 to 150%	0 to 5.277	2.23%	4.46%
Vertical Acceleration (Load Factor)	-1.5 to 3.5g	Undefined	0.16g	0.32g
Collective Stick Position	0 to 100%	± 6.7	3.2%	6.4%
Lateral Stick Position	± 50%	Undefined	3.2%	6.4%
Longitudinal Stick Position	± 50%	± 7.0	3.2%	6.4%
Pedal Position	+ 50%	Undefined	3.2%	6.4%
Ice Rate	0 to 1.0 gm/m^3	1.0 to 5.0	0.04 gm/m^3	0.08 gm/m^3
Altitude Rate	+ 6000 fpm	± 10	46.8 fpm	93.6 fpm
Vertical Impact Acceleration	± 150g	± 10	2.4g	7.0g
Lateral Impact Acceleration	± 150g	± 10	2.4g	7.0g
Longtudinal Impact Acceleration	± 150g	± 10	2.4g	7.0g
Spare DC				
Spare DC				
Analog Self Test	0 to 5.1 VDC	0 to 5.1	N/A	N/A

TABLE 2. BLACK HAWK (UH-60A) PARAMETER LIST (AC ANALOGS)

PARAMETER	DATA RANGE	SIGNAL RANGE	RESOLUTION	LIMIT EXCEEDANCE
Heading	0 to 360°	0 to 11.8 VAC, 400 Hz	1.8°	1.8°
Roll Attitude	± 180°	0 to 11.8 VAC, 400 Hz	0.9°	1.8°
Pitch Attitude	± 82°	0 to 11.8 VAC, 400 Hz	0.9°	1.8°
Stabilator Indicator	+10° to -45°	0 to 11.8 VAC, 400 Hz	3.2% of total stroke	6.4% of total stroke
Spare Synchro				
Spare Synchro				
Spare Synchro				
Synchro Self Test				
Rotor RPM	0 to 130%	0 to 14,326 Hz	2%	4% @ 100%
Engine #1 RPM (NG)	0 to 110%	0 to 2,349.3 Hz	1.5% 0.38%	3.0% @ 100% 0.76% @ 50%
Engine #2 RPM (NG)	0 to 110%	0 to 2,349.3 Hz	1.5% 0.38%	3.0% @ 100% 0.76% @ 50%
Spare Frequency				
Frequency Self Test	2400 Hz	2400 Hz		

TABLE 3. BLACK HAWK (UH-60A) PARAMETER LIST (DISCRETES)

PARAMETER	DATA RANGE	SIGNAL RANGE (VDC)	RESOLUTION	LIMIT EXCEEDANCE
Altitude (9 Bit Grey Code)	-100 to 50,000 ft	2.5 (low) 9.0 (high)	Any Change	Any Change
SAS/FPS Computer Fault	Fault Normal	0 to 2 (50 msec) 10	Any Change	Any Change
SAS Warning	Pressure Off Pressure On	28 0	Any Change	Any Change
Main Fire Dectection	Fire No Fire	28 0	Any Change	Any Change
Chip Detection Engine #1	Chips No Chips	28 0	Any Change	Any Change
Chip Detection Engine #2	Chips No Chips	28 0	Any Change	Any Change
Hydraulic Pressure Engine #1	Pressure Low Pressure Norm	28 0	Any Change	Any Change
Hydraulic Pressure Engine #2	Pressure Low Pressure Norm	28 0	Any Change	Any Change
Hydraulic Pressure APU	Pump On Pump Off	28 0	Any Change	Any Change
Spare 28V (20)	---	---		
Spare Shunt (8)	---	---		
Event (Shunt)	N/A	---	Any Change	Any Change
MRU (Shunt)	N/A	---	Any Change	Any Change
PGU (Shunt)	N/A	---	Any Change	Any Change

TABLE 4. PRELIMINARY AAH PARAMETER LIST

PARAMETER	SIGNAL TYPE	DATA RANGE	SIGNAL RANGE	COMMENTS
Airspeed	DC Analog	0 to 200k	0 to 10 VDC	
Heading	AC Synchro	0 to 360°	0 to 11.8 VAC, 400 Hz	
Pressure Altitude	DC Analog	Undefined	0 to 10 VDC	From air data system
Vertical Acceleration	DC Analog	-1.5 to 3.5g	Undefined	Must Provide Sensor
Pitch Attitude	DC Analog	Undefined	+ 10 VDC	
Roll Attitude	DC Analog	Undefined	+ 10 VDC	
Engine Torque	DC Analog	Undefined	0 to 8 VDC	
Rotor RPM	Frequency	0 to 100%	0 to 1348 Hz	
Engine RPM	Frequency	0 to 100%	0 to 1396.76 Hz	
Fire Detection	Discrete	Fire No Fire	Closed Open	Switch Closure
Chip Detectors	Discrete	Chips No Chips	Closed Open	Switch Closure
Hydraulic System Pressure	Discrete	Pressure Low Pressure Norm	Closed Open	Switch Closure
Lateral Stick Position	DC Analog	± 4.5 in	± 10 VDC	
Longitudinal Stick Position	DC Analog	± 5 in	± 10 VDC	
Collective Stick Position	DC Analog	± 6 in	± 10 VDC	
Pedal Position	DC Analog	+ 4.5 in	+ 10 VDC	
Altitude (9 Bit Grey Code)	Discrete	-100 to 50,000 ft	Lo= 2.5 VDC Hi= 9.0 VDC	
Vertical Impact Acceleration	DC Analog	± 150g	± 10 VDC	Must Provide Sensor
Lateral Impact Acceleration	DC Analog	± 150g	± 10 VDC	Must Provide Sensor
Longitudinal Impact Acceleration	DC Analog	± 150g	± 10 VDC	Must Provide Sensor
Stabilator Position	AC Synchro	+10° to -45°	0 to 11.8 VAC, 400 Hz	

(3) Completely Solid-State Electronics

The AIRS signal conditioner, microprocessor, and recording unit are completely solid-state. Even power switching, which is essential to AIRS automatic operation, is accomplished using solid-state techniques at very little continuous power drain.

(4) Nonvolatile Solid-State Memory

Electrically alterable read-only memory systems (EAROM's) have been tested and qualified over the full military temperature range. Several Hamilton Standard aviation products currently utilize EAROM's. These devices will in themselves be hermetically sealed and will be capable of shock levels in excess of the shock level requirements for the protected memory module.

Bubble memories offer significant advantages over EAROM's in terms of cost, size, and weight for the large memory capacities. These devices are not proven for use in military applications at this time but will be considered for future AIRS applications.

(5) Memory Module Survivability Per TSO-C51a (See Reference 2)

Techniques for survivability per this specification are in hand. A combination of water boil-off and use of intumescent coatings will allow thermal exposures well in excess of the specification requirements.

(6) Automatic Operation With Aircraft Power Actuation

A signal obtained from any switching element which is routinely engaged when starting the aircraft can be used to automatically switch on the AIRS. Power will be controlled using solid-state switching directly from the aircraft battery.

(7) In-Flight Emergency Shutdown Procedures or Transmission Seizure Shall Not Interrupt Power to The AIRS Unit

Not routing AIRS power to the normal circuit breaker panel and not allowing the AIRS unit to shut itself off until a suitable time delay after rotor speed has dropped below a predetermined value will always preclude power being interrupted to the AIRS electronics.

(8) Data Retrieval Without Removal of Any AIRS Components From The Aircraft Except When Airborne Unit is Rendered Inoperable

Access to the AIRS data memory will be via the microprocessor upon command from a portable ground unit after plugging directly into the in-place AIRS unit. Data can then be read out and recorded.

(9) Built-In Test Capability

The microprocessor allows a very high level of built-in test capability. Such proven techniques as periodically inputting calibration signals, timing out the execution of the processor mainline program, and having a processor read information from the data memory after writing will allow a very high level of built-in test.

(10) Compatibility With Helicopter Vibration Noise and Operational Environment

There does not appear to be any problem with regard to the design and production of AIRS hardware to meet the helicopter environment.

(11) Compact Packaging of Airborne Unit

Advances in microprocessor design and manufacture and in memory systems design, along with higher orders of circuit integration, will allow compact packaging of the AIRS airborne unit. Two hundred-seven cubic inches of volume is an achievable goal for the AIRS airborne unit.

(12) The Portable Ground Unit (PGU) Shall Be Commercially Available

A number of versions of data recorder terminals called PGUs for AIRS are available from industry. The use of standard techniques for transmitting digital data from the AIRS unit makes possible the potential use of any one of these PGU types.

Design Goals

(1) System Design for Minimum Cost, Weight and Size

Escalation of the constant dollar cost of AIRS production hardware would adversly affect the AIRS program. Cost control must be emphasized. The size and weight projections as given in Reference 1 still appear as valid goals.

(2) Maximum Use of Existing Aircraft Circuits and Sensors

For the UH-60A, approximately 75% of the input signals can be used directly without the need for special AIRS sensors. Techniques are well in hand to provide the necessary electrical isolation between AIRS input circuits and the various signal sources.

(3) Maintenance Free

With the built-in test capability and completely solid-state construction, the unit will not require any recurrent periodic maintenance.

(4) MTBF Greater Than 5000 Hours

Preliminary calculations of mean-time-between-failures still indicate that greater than 5000 hours can be achieved with today's solid-state component technology.

(5) Ease of Installation and Removal From Aircraft

Once access is gained to any of the AIRS line replaceable units, any unit can be quickly removed and replaced.

(6) Minimum Ground Based Hardware and Software For Data Retrieval

Versions of portable ground units for data extraction are available commercially at reasonable cost. In addition, transmission, reception, and inputting to a central computing system can be accomplished using available hardware elements. Basic software to accomplish engineering units conversion and plot/print routines are used routinely by the industry.

(7) Data Output Compatible With General-Purpose Computer Systems Such as That at the U.S. Army Safety Center, Fort Rucker, Alabama

Data from AIRS can be received or read and stored in such computer systems with available peripherals and standard software elements.

(8) Ability to Record Secondary Crash Impact For up to 10 Seconds After Initial Crash Impact

The most cost effective technique for obtaining secondary crash impact data is to rely on the essential battery in the aircraft. A short, protected, and armored cable from the AIRS unit to the battery should allow AIRS operation through high impact forces. In addition, ruggedization of the overall AIRS unit to withstand impact shocks up to 150g appears to be an achievable goal.

Utilization of an internal battery source for this purpose does not appear to be the best way of maintaining power. This technique would require periodic maintenance to check and/or replace the internal battery source.

(9) Average Flight Time Data Storage of 30 Minutes

The analysis of actual helicopter flight data indicates that 32,000 bits of memory should allow an average of 30 minutes of flight time to be available in memory. Advancements in memory chip technology will permit expanded memory capability within the same volume but at increased cost.

(10) Hardware and Software Compatible With More Than One Aircraft

It is technically feasible that a hardware/software package could be developed such that one package would be interchangeable between two (or more) similar aircraft types (for example, the Army BLACK HAWK and the AAH).

SYSTEM DESIGN GUIDELINES FOR AIRS

The following defines the signal inputs, outputs, and performance guidelines for AIRS. The AIRS can accommodate signals from a number of aircraft types and includes signal conditioner flexibility which allows adaptability to other aircraft.

The AIRS unit samples various analog and discrete data under microprocessor program control. It compares the sampled data against fixed and floating limits. It also outputs properly formatted data to an Electrically Alterable Read Only Memory (EAROM) when limits are exceeded or at a minimum output rate as applicable. The data is read later on the ground using a Portable Ground Unit (PGU) which dumps the data onto a cassette contained in the PGU. Two display drivers are included in the AIRS unit to energize cockpit displays: one to indicate a requirement to dump data and one to indicate an AIRS unit fault.

An additional output interface exists to allow real-time readout of selected parameters for maintenance purposes only.

The following documents apply to the AIRS design guidelines.

EIA Standard RS-232-C, Interface between data terminal equipment and data communication equipment employing serial binary data interchanges.

MIL-STD-704C, Aircraft Electrical Power, Characteristics and Utilization of (except as amended herein).

MIL-STD-461A, Electromagnetic Interference Characteristics, Requirements for Equipment (except as amended herein).

MIL-E-5400M, Class 1A Electronic Equipment, Airborne, General Specification for (except as amended herein). (See Table 5.)

FAR 37.150, TSO-C51a, Federal Aviation Regulation, Crash Survivability Requirements for Commercial Transport (except as amended herein - see Table 6.)

TABLE 5. SUMMARY MIL-E-5400M CLASS IA FOR HELICOPTERS

Altitude	0 to 30,000 feet	
Temperature	Continuous operation	-54°C to +55°C
	Intermittent	30 min. at +71°C
	Nonoperating	-60°C to +85°C
Vibration	20 to 30 Hz	2g
	52 to 2000 Hz	5g
Shock	Operating	15g for 11 msec
	Mount (Crash Safety)	30g for 11 msec

TABLE 6. SUMMARY OF MAJOR CRASH SURVIVAL REQUIREMENTS OF TSO-C51a

Impact	1000g half sine for 5 milliseconds.
Penetration	500 pound weight dropped from 10 feet on 0.05 square inch area.
Static Crush	5000 pounds continuous
Fire	1100°C on 50% of outside area for 30 minutes if near fuel tanks, 15 minutes if not near fuel tanks.
Water	Immersed in sea water for 36 hours.

General Requirements

The AIRS will fit within an envelope of 207 cubic inches or less with width, height, and length less than 7 inches and will weigh less than 9.25 pounds (uninstalled).

The AIRS will consume less than 25 watts average.

The AIRS will endure the following temperature ranges as specified:

Continuous operation: -54°C to +55°C

Intermittent operation: 30 minutes @ 71°C

Nonoperating: -60°C to +85°C

The crash survivability of the AIRS armored module shall be per FAR 37.150, TSO-C51a, except immersion time in salt water is increased to 4 weeks.

The AIRS electronics unit shall be designed such that the system will function through a 150g, 10-millisecond duration impact in any axis.

The requirements of MIL-STD-461A apply except as noted below. MIL-STD-704C should not be specified in its entirety with regard to power. The AIRS will be powered from a dedicated 28-volt DC battery bus. Power will not be interrupted during normal or emergency conditions except for cause associated with an aircraft mishap. A keyed connector will be used at the battery relay box. Because of the above, certain requirements of MIL-STD-704C and -461A for transient overvoltage, polarity reversal, and EMI susceptibility with regard to input power should not be invoked. By not invoking these requirements, the size, weight, and cost of the AIRS electronics can be minimized.

Signal Processing Requirements

DC Analogs

Fifteen DC analog inputs will be provided. Three ranges ($\pm$ 5, $\pm$ 10, $\pm$ 15) of DC voltages will be handled by resistor value changes on the necessary channels. These channels will accept 5K potentiometer type sensor inputs utilizing the $\pm$ 10 VDC AIRS sensor excitation output.

Input impedance for each analog channel will be greater than 100K ohms and resistive in nature.

Input signals will be differentially received and retain specified accuracies with $\pm$ 5 VDC or 5 VRMS at 400 Hz common-mode voltage applied.

Each channel will have a single-pole low-pass filter with a cutoff frequency suitable for the input signal on that channel, nominally 10 hertz.

The root sum squared (RSS) summation of all errors due to manufacturing tolerances of components, offsets, temperature effects, common mode voltages, etc., will represent less than 2% full scale.

Synchro Inputs

Seven standard three-wire synchro inputs can be accommodated.

Input impedance for each synchro channel will be greater than 20K ohms.

Input signals will be differentially received and retain specified accuracies with ± 5 VDC or 5 VRMS at 400 Hz common-mode voltage applied.

The synchro input will be synchronously demodulated. The output will be filtered by a single-pole low-pass filter with a 3-db point at 6 Hz ± 5%.

The RSS summation of all errors due to manufacturing tolerances of components, offset, temperature effects, common-mode voltages, etc., represent less than 2% of full scale.

Frequency Inputs

Five ranges of frequency will be accommodated as given below. A maximum of four frequency inputs will be provided: the 7-90 Hz input will be an approximate sine wave, the rest can be sine waves, square waves, or pulses with a minimum pulse duration of 10 μs. Input peak amplitude will be between 0.5V and 70V. Four inputs will be accommodated. Frequency ranges are:

7 - 90 Hz

160 - 400 Hz

500 - 1,500 Hz

250 - 3,000 Hz

5,000 - 13,000 Hz

Input impedance for each frequency channel will be greater than 100K ohms and will be resistive in nature.

Input signals will be differentially received and retain specified accuracies with ± 5 VDC or 5 VRMS at 400 Hz common-mode voltage applied.

Discrete Inputs

Two types of discrete (logic zero/logic one) inputs will be accepted as defined below. Forty-eight discrete signals will be accommodated.

Discrete Type	Logic Zero	Logic One
Shunt:	Greater than 100K ohms	Less than 375 ohms
Series:	Greater than 18.5 VDC	Less than 1.9 VDC

The discretes will be received single-ended and will be referenced to a common 28V power return bus.

An input filter will be provided for all discrete inputs consisting of a low-pass filter with a single pole at 30 Hz ± 50%.

The input impedance will be greater than 100K ohms and resistive in nature.

Computer Data Input

Twenty-four channels of analog multiplexing will be provided which are compatible with the outputs of the signal conditioners.

The output of the multiplexer will be digitized by a 10 bit analog to digital (A/D) converter. The A/D conversion time will be 20 μs, max. Addressing of the multiplexer will be random in nature, under microprocessor control. The A/D converter will provide an "A/D-complete" signal. The accuracy from analog multiplexer input to A/D digital output will be $\pm$ 1% of the input signal. This error will include all sources of error such as manufacturing tolerances, temperature effects, offsets, channel cross-talk, etc.

A discrete multiplexer will be provided that is capable of accepting 48 input signals from the discrete signal conditioners. The discrete multiplexer will be randomly addressable under microprocessor program control.

Microprocessor and Support Circuitry

A microprocessor will be provided to handle the data for compression, built-in-test, and other software controlled functions.

A clock will be provided with countdown circuitry as required for microprocessor operation and input/output (I/O) control.

Data/control bus latches and drivers will be provided as required for proper operation of the microprocessor and proper I/O control.

The appropriate computer I/O control logic will be provided to interface with the input signals and provide the output signals as well as multiplexer control signals.

A scratch-pad memory with 1536 bytes of random access memory (RAM) will be provided.

8192 bytes of read only memory (ROM) will be provided for program storage.

Thirty-two thousand bits of EAROM will be provided for nonvolatile data storage. EAROM read/write control and power strobing must be available under processor control to minimize EAROM power dissipation.

A watchdog timer, reset under microprocessor control, will be provided. It's output will cause the BIT output to activate directly.

Data Outputs

A two-wire RS232-compatible input and output will be provided so that, via an input discrete, the data stored in the EAROM will be read out sequentially from a given starting address to an external Portable Ground Unit (PGU). The

RS232 input will be used for handshaking functions in conjunction with the PGU and data read-back to verify proper EAROM transcription.

A magnetic latching indicator will be provided to indicate a unit failure. The indicator will be tripped by the microprocessor based on software diagnostics or directly by the watchdog timer. The indicator is excited directly by 28 VDC and represents a 50 ma current load. In addition, a discrete drive will be provided for remote annunciation.

A magnetic latching indicator (optional) can also be provided to indicate the occurrence of an unusual event. This can be used to indicate that some limit has been exceeded such as an airframe overstress or a rotor overspeed. This occurrence can be protected in memory so that ground personnel can determine what occurred and what resultant action is required.

An output interface will be provided to allow a Burroughs self-scan display or equivalent to be driven by the real-time data under microprocessor control. To minimize the memory overhead carried in the unit for readout, as well as any special interface, the memory required for this function will be external to the AIRS. The essential data and control busses will be provided, and adequately buffered, to prevent the introduction of noise into the unit. In addition, five discretes will be input to the discrete signal conditioners to allow parameter identification for the maintenance readout.

An input signal equivalent to a mid-range analog signal will be provided. Two discretes will also be provided, one wired as a "1" and one as a "0".

Power Supply

A regulated power supply will be provided which is energized from the 28 VDC aircraft bus per MIL-STD-704D, as modified herein. The power supply will provide the necessary excitation for the AIRS internal circuitry plus the following output for sensor excitation: $\pm$ 10 VDC at 50 ma/side with a tolerance of $\pm$ 1%.

The operation of the AIRS is completely automatic to preclude manual defeat of the system or depletion of the battery during aircraft downtime. Actuation of any engine start switch will provide power to the AIRS unit directly from the battery. The AIRS unit will run a self test and then initialize itself for operation. Recording will begin when either engine or the rotor is at 80% rpm or higher. Recording will continue until the shutdown conditions are met for a period of 2 to 3 minutes. These shutdown conditions are rotor and at least one engine below 20% rpm. The presence of these conditions for 2 to 3 minutes clearly indicate that the aircraft is no longer flying. Once these conditions have been met, the processor then stops recording, performs an orderly shutdown, and then removes power from the unit.

A manual start is provided in addition to the start switch inputs for use in conjunction with a Portable Ground Unit (PGU) or a Maintenance Readout Unit (MRU).

MEMORY TECHNOLOGY EVALUATION

The AIRS design concept relies on storing digital data in a crash protected solid-state memory storage device which is nonvolatile, able to withstand rigorous environmental conditions, and provides sufficient data storage capacity for recreation of aircraft flight profiles.

Hamilton Standard has evaluated various nonvolatile solid-state memory devices available in the industry, including magnetic bubble memory and Electrically Alterable Read Only Memory (EAROM) devices. A third promising technology in the category of nonvolatile memory systems is the Electrically Erasable Programmable Read Only Memory (E^2PROM).

The memory technology evaluation concentrated on factors such as:

* Production Availability
* Electrical Characteristics
* Environmental Characteristics
* Complexity
* Cost

BUBBLE MEMORY DEVICES

In 1978, Hamilton Standard procured and tested bubble devices manufactured by Western Electric and Texas Instruments. The primary thrust of these tests was temperature characterization during operation and under storage conditions. Satisfactory operation was achieved over the range of 0°C to +60°C while data retention over the range of -50°C to +100°C proved satisfactory. The failure of the devices to even approach operation over the full military temperature range negated consideration of these devices in the AIRS development program. Western Electric did indicate confidence that, with additional development effort and time, a mil-temperature device could be achieved.

During the latter part of 1978, Rockwell performed extended temperature testing of a 256K bit device (RBM 256). Experiments with bias field and drive field changes were accomplished to compensate somewhat for changes in temperature.[3] Their current devices were found to operate over a temperature range of -25°C to +75°C. Rockwell reported gaining valuable information that could lead to improved bubble memories and "---eventual militarization of the bubble device".

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3. NADC 78170-50, BUBBLE MEMORY DEVICE CHARACTERIZATION STUDY, November 1979, Rockwell International, Autonetics Strategic Systems Division, P.O. Box 4192, 3370 Miraloma Ave., Anaheim, Calif. 92803.

During this same period, Texas Instruments published a report[4] discussing the effects of temperature on TI's 254K bit magnetic bubble memory device. The nominal operating temperature range was found to be -25°C to +75°C with a storage temperature range of -50°C to +110°C. TI indicated that there were several areas which were being examined in order to expand the temperature limits of the device and indicated that the possibility exists that a mil-temperature device could be developed in the mid-1980's.

The potentially large market for bubble memory devices, especially commercial, has prompted several other manufacturers to invest development time and money in this technology. INTEL Corporation has two 1-megabit devices which differ from the Western Electric, TI, and Rockwell devices only in their frequency of operation. National Semiconductor will have a 256K bit bubble device in full production by mid-1981 and will also be working on a 1-megabit device. Motorola is second sourcing Rockwell's 256K bit device (already in production at Rockwell) and will be evaluation tested by Motorola in late 1980. Both Rockwell and Motorola are working on a 1-megabit bubble device but as yet have no compatibility agreements. Rockwell's 256K and 1-megabit device will be interchangeable.

Western Electric is presently producing a 256K bit serial loop device and is working on a 250K bit major/minor loop bubble memory.

Texas Instruments has the largest family of devices including 1-megabit, 500K bit, and 250K bit bubbles which are interchangeable with the 92K bit device tested by Hamilton Standard in 1978.

The largest bubble device available contains a 1-megabit memory and is produced by both INTEL (two versions) and Texas Instruments. Rockwell will be evaluating a 1-megabit device late-1980 while Motorola plans to be evaluating theirs in 1981. Texas Instruments makes 1/2-megabit and 1/4-megabit devices, both of which are interchangeable with the 1-megabit bubble and 92K bit bubble. National Semiconductor, Rockwell, Motorola, and Hitachi each have a 1/4-megabit device while Western Elecrtric has a 272K bit serial bubble and is working on a 250K major/minor loop device. Hitachi plans 1- and 4-megabit devices to be available sometime in late 1982 or early 1983.

All bubble devices require extensive interface circuitry. The manufacturers are all developing their own custom integrated control chips.

Power requirements of the bubble memories themselves range from 450 milliwatts for the Hitachi 64K bit device to 1.9 watts for each of the two INTEL bubbles.

Voltage requirements were not available for the Hitachi bubble memories. Western Electric requires +5 VDC and $\pm$15 VDC for the 272K bit device and +5 VDC and $\pm$ 12 VDC for the 250K bit device. Motorola, National Semiconducter, and INTEL use +5 VDC and +12 VDC while TI and Rockwell use +5 VDC and $\pm$12 VDC.

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4. NADC 78175-50, BUBBLE MEMORY DEVICE CHARACTERIZATION STUDY, February 1980, Texas Instruments Inc., Central Research Lab., 13500 North Central Expressway, Dallas, Texas 75265.

Bubble write times are dependent upon frequency of operation. INTEL's write time is typically 17 μs/8 bits for their 7110 and 58.4 μs/8 bits for the 7112. National Semiconductor takes 80 μs/8 bits for their 256K device while TI requires approximately 50 μs/8 bits for their 1-megabit device. Rockwell's 256K device write time is 52.8 μs/8 bits. Write time for their 1-megabit bubble was not available. Motorola is a second source for the Rockwell RBM 256. Timing information for the 1-megabit part was not available.

Temperataure ranges are a serious drawback for current bubble memory technology. Operating range is on the order of 0°C to 70°C, with the largest storage temperature range being -50°C to 100°C claimed by Rockwell and Motorola. The bubble memory technology status, as of December 1980, is summarized in Table 7.

ELECTRICALLY ALTERABLE READ ONLY MEMORY (EAROM)

EAROM's are solid-state nonvolatile memory devices. They can be in-circuit programmed or erased. The memory element is the metal-nitride-oxide-semiconductor (MNOS) transistor. It is a basic MOS transistor which has had the gate oxide layer replaced by a silicon dioxide-silicon nitride sandwich. The silicon dioxide is made 25Å (angstroms) thick to allow charge to tunnel through at gate voltages of 25 to 30. When electrons tunnel through the oxide layer, they become trapped at the nitride-oxide interface which alters the threshold of the device. The transistor can then be read to determine the logic level stored.

Westinghouse makes several Block Oriented Random Access Memories (BORAM's). They are a 2K and an 8K bit chip with 32K and 131K bit chips 1 to 2 years away. Westinghouse packages these in hybrids which can house up to 16 chips. Sperry Univac also has an 8K BORAM available and is looking into manufacturing a 65K device.

Nitron, General Instruments (GI), and National Cash Register (NCR) have 1K X 4 and 2K X 4 EAROM's available; however, all of their 2K X 4 devices are difficult to interface because of the necessity of pulsed power supplies. Seimans has a 1K X 8 device which also uses pulsed power supplies; they may look at larger devices in the future. All of the aforementioned EAROM's have storage temperature ranges of -55^{o} to $125^{o}C$. NCR's devices would require outside screening to achieve the above temperature range. NCR, GI, and Nitron are willing to sell dies to be placed in a hybrid; however, the dies would not have been tested over the entire mil temperature ranges. GI and Nitron expressed an interest in building a tested hybrid.

MNOS EAROM memories have a limited lifetime as a result of degradation of the nitride film during write cycles. These devices currently are limited to 10^5 erase-write cycles per word. Some device manufacturers are now claiming further improvements to 10^6 cycles and higher. However, in the AIRS application, an average erase-write cycle would occur less than twice per location per hour thus providing a memory lifetime in the tens of thousands of operating hours.

TABLE 7. BUBBLE MEMORY TECHNOLOGY STATUS (11/6/80)

VENDOR	PART NUMBER	STORAGE CAPACITY (IN BITS)	DESIGN	ELECTRICAL CHARACTERISTICS			TEMPERATURE CHARACTERISTICS		SIZE (IN INCHES)	I/O PINS	AVAIL-ABILITY	COST
				ACCESS TIME	VOLTAGES REQUIRED	POWER DISSIPATION	OPERATING	STORAGE				
Texas Instruments (Note 1)	TIB 1000	1MEG	--	11.2MS	+5, ± 12	1.2W	0°C to 70°C	-40°C to+85°C	1.1x1.4x0.4	24	4 Wks	$200 in 1981
	TIB-0500	1/2MEG	Page Swap/ Replicate	11.2MS	+5, ± 12	1.2W	0°C to 70°C	-40°C to+85°C	1.1x1.4x0.4	24	4 Wks	$125 in 1981
	TIB-0250	1/4MEG	Page Swap/ Replicate	6.1MS	+5, ± 12	1.2W	0°C to 70°C	-40°C to+85°C	1.1x1.4x0.4	24	4 Wks	$100 in 1981
	TIB-0203	92K	Major/Minor	4MS	+5, ± 12	0.7W	0°C to 70°C	-40°C to+85°C	1.1x1.4x0.4	14	4 Wks	$50 now
Intel (Note 2)	7110	1MEG	Block Replicate 512 Bit Page/2048 Pages	40MS (60 KHZ Nom. Data Rate)	+5, + 12	1.9W	0°C to 70°C -20°C to 85°C Future Poss.	-40°C to+100°C	1.5x1.7x0.5	20	Now	$2,195 with Proto-board
	7112	1MEG	Block Replicate	20MS (136 KHZ Nom Data Rate)	+5, + 12	1.9W	0° to +50°C	-40°C to+100°C	1.5x1.7x0.5	20	1981	Unknown
National Semi-Conductor (Note 3)	NBM2256	256K	Major/Minor 256 x 1024	7MS	+5, +12	Unknown	0°C to +70°C	-40°C to+100°C	1.1x1.02x0.34	Unknown	Full Prod Mid 1981	$500
	- -	1MEG	Major/Minor	1st 16 Bytes write every 10μs 80 μs/word thereafter	+5, +12	Unknown	0°C to +70°C	-40°C to+100°C	1.1x1.02x0.34	Unknown	≈Mid 1981	Unknown
Rockwell (Note 4)	RBM256	256K	260 loops x 1024 bits	4MS	+5, ±12	1W	-10°C to+70°C	-50°C to+100°C	1.2x1.2	18	In Pro-duction	$410
	RBM411	1MEG	Unknown	Unknown	Unknown	Unknown	-10°C to+70°C	-50°C to+100°C	1.2x1.2	18	DEC 1980	$1,455

TABLE 7. BUBBLE MEMORY TECHNOLOGY STATUS (CONTINUED)

VENDOR	PART NUMBER	STORAGE CAPACITY (IN BITS)	DESIGN	ELECTRICAL CHARACTERISTICS			TEMPERATURE CHARACTERISTICS		SIZE (IN INCHES)	I/O PINS	AVAIL-ABILITY	COST
				ACCESS TIME	VOLTAGES REQUIRED	POWER DISSIPATION	OPERATING	STORAGE				
Motorola (Note 5)	RBM256	256K	260 Loops x 1024 bits	4MS	+5, ± 12	1W	-10°C to +70°C	-50°C to +100°C	1.2 x 1.2	18	Sampling now	$500
	MBM1000	1MEG	Major/Minor	10MS	Unknown	Unknown	0°C to +50°C	-30°C to +100°C	Unknown	Unknown	Sampling in 1981	Unknown
Western Electric (Note 6)	- - -	272K	(4)68K bit loops	650MS	+5, ± 15	1W	0°C to +70°C (-30°C to +60°C)	-40°C to +80°C (-30°C to +120°C)	1.2x2.5x0.7	Unknown	Now	Unknown
	29C	250K	Major/Minor	6MS	+5, ± 12	800MW	0°C to +60°C	-40°C to +85°C	1.5x2.0x0.6	Unknown	Unknown	Unknown
Hitachi (Note 7)	B0G0101	64K	128 Loops x 535 Bits	5MS	Unknown	450MW	0°C to +50°C	-40°C to +85°C	Unknown	18	Unknown	Unknown
	H4701B	256K	256 Loops x 1135 Bits	7MS	Unknown	800MW	0°C to +50°C	-40°C to +85°C	1.0x1.0x0.5	20	Unknown	Unknown

NOTES:

1. TI does not expect mil-temperature bubbles before 1982. TI 1 MEG device has 34 BYTE page only, 92K device has 18 BYTE page only. After page is written in either device, it takes 80 microseconds to write 8 Bits. All devices are interfaced by six (6) custom integrated circuit devices.
2. Intel does not foresee a mil-temperature device. The 7110 One MEG devices employ 40 x 8 FIFO writes at 1.6 μs/8 bits @4 MHZ. Thereafter, writes at 117 μs/word. The 7112 one MEG device operates at 117 μs/8bits to bubble. Both devices are interfaced by six (6) custom integrated circuit devices.
3. First 16 bits are written every 10 μs, thereafter writes at 80 μs/word. Bubble is paralleling with an external shift register. NS does not plan to develop a mil temperature device. NS interfaces the device with 5 custom large scale integration (LSI) devices.
4. Both the 256K and 1 MEG devices are interchangeable. Rockwell is not planning a mil temperature device. Rockwell is presently designing custom LSI devices to interface the bubble memories.
5. Motorola is second source for Rockwell 256K device. The Motorola 1 MEG device is not interchangeable with the 256K device and they do not have agreement for second source to Rockwell. Motorola will use custom controller being developed by Rockwell plus other custom LSI's being developed by Motorola to interface to bubbles.
6. W.E. uses one 8 1/2 x 11 controller board and one 8 1/2 x 11 bubble board to form complete system for 272K device. Presently developing custom LSI's for 250K devices. WE is also looking at larger devices.
7. Hitachi is not selling the 64K device because of interest in 256K device. They plan to start work in 1981 on a 1 MEG device and will have a 4 MEG device in the 1982-1983 time frame for which they are looking for second source. Interface to all devices will be custom designed integrated circuits.

Hamilton Standard used the Westinghouse 32K bit hybrid BORAM for Phase 1 and II AIRS testing while independently developing a 32K bit hybrid device using both NCR's 2451 (4K) chips and GI's ER3400 (4K) chips.

The hybrid circuit developed by Hamilton Standard has the advantage of requiring less support circuitry for operation while providing a simplified interface in comparison to the Westinghouse BORAM unit. The areas of simplification include direct parallel input of data in lieu of parallel to serial conversion in the BORAM, direct read/write capability in comparison to the block data read/write (256 bits) in the BORAM, and no level conversions whereas BORAM requires TTL to CMOS level conversions. The results of this simplified operation afford a 50% reduction in support hardware requirements and an attendant lower cost.

Westinghouse makes the highest density family of devices, ranging from 2K and 8K bits/chip with 32K and 131K bit/chips planned for 1981/1982. Sperry Univac currently has an 8K BORAM, while General Instrument, NCR, and Nitron have 8K and 4K EAROM's available.

The Westinghouse and Sperry Univac BORAM devices require a considerable amount of interface circuitry for timing and signal voltage level control. All of the 8K EAROM's are also difficult to interface because they require the power supplies to be pulsed during a write or erase operation. The 4K devices from GI, NCR and Nitron are the easiest to interface since they are static, T^2L compatible devices (with resistor pull-ups) and do not require pulsed power supplies.

The Westinghouse BORAM's dissipate the least amount of power, typically 375 mw for the 2K and 8K devices. The 4K devices from Nitron and NCR require approximately 400 mw, while the 4K EAROM from GI dissipates about 570 mw. The GI, NCR and Nitron 8K EAROM's dissipate the most power, typically 650 mw.

All of the EAROM's require multiple power supplies, from two for the Sperry Univac device to four for the GI, NCR, Nitron and Seimans 8K devices. The 4K EAROM's require three power supplies each as do the family of Westinghouse BORAM's.

All devices surveyed will store data from -55°C to at least 125°C. Only NCR and Nitron had operating ranges of 0-70°C while the others are rated at -55°C to 125°C.

The Seimans 8K device is the slowest, taking 1 second to chip erase and 10-20 ms/word to write. The same manufacturer's 4K devices require 10 ms to word or chip erase and only 1 ms/word to write data. The Westinghouse BORAM's take on the order of 236 μs to write 32 bits and 1 ms to chip erase. Sperry Univac specifies typically 500 μs to write and 500 μs to erase a block of data. Only GI and Sperry Univac plan to develop larger devices. The EAROM technology status, as of December 1980, is summarized in Table 8.

TABLE 8. EAROM/BORAM TECHNOLOGY STATUS

VENDOR	PART NUMBER	STORAGE CAPACITY (IN BITS)	DESIGN	ELECTRICAL CHARACTERISTICS				TEMPERATURE CHARACTERISTICS		I/O PINS	AVAILABILITY	COST	INTERFACE COMPLEXITY
				ACCESS TIME	READ/ WRITE CYCLES	VOLTAGES REQUIRED	POWER DISSIPATION	OPERATING	STORAGE				
General Instruments (Note 1)	3400	4096	1024x4	12MS	10^5	+5,-12,-30	570MW	-55°C to +125°C	-55°C to +125°C	22	Off the Shelf	$36.66	- - -
	2810	8192	2048x4	110MS	10^5	±5,-14,-24	650MW	-55°C to +125°C	-55°C to +125°C	24	2 to 3 weeks	$39.74	Pulsed power supplies
Nitron (Note 2)	7810	8192	2048x4	110MS	10^5	±5,-14,-23	650MW	-55°C to +125°C	-55°C to +125°C	24	2 to 4 weeks	$21.85	Pulsed power supplies
	7451	4096	1024x4	12MS	10^5	+5,-12,-30	>400MW Preselected	-55°C to+125°C	-55°C to+125°C	22	4th qtr 1981	$17.25	- - -
National Cash Register (Note 3)	2451	4096	1024x4	12MS	10^5	+5,-12,-30	450MW	0°C to 70°C	-55°C to+125°C	22	8 to 10 weeks	$22.00	- - -
	2810	8192	2048x4	125MS	10^6	±5,-14,-23	650MW	0°C to 70°C	-55°C to+125°C	24	8 to 10 weeks	$25.00	Pulsed power supplies
	2401	4096	1024x4	120MS	10^6	+5,-15,-23	>400MW	0°C to 70°C	-55°C to+125°C	24	16 to 20 weeks	$18.00	Pulsed power supplies
Seimans	SAB2808	8192	1024x8	60sec erase 50MS write	10^3	±5,+12,+33, +25	400MW	0°C to 70°C	Unknown	24	Unknown	Unknown	Pulsed power supplies
Westinghouse (Note 4)	6002C	2048	64x32	5 μs	10^5	±5,+5,-20	< 375MW	-55°C to+125°C	-65°C to+150°C	24 (Hybrid)	12 to 15 weeks	$3K/ System	4.5x5.5 P.C. Card
	6008	8192	64x128	5 μs	10^5	±5,+5,-20	< 375MW	-55°C to+125°C	-65°C to+150°C	24 (Hybrid)	12 to 15 weeks	$3.7K/ System	4.5x5.5 P.C. Card
	6032	32K	256x128	10 μs	10^5	±5,+5,-20	Unknown	-55°C to+125°C	-65°C to+150°C	24 (Hybrid)	1 Year	Unknown	4.5x5.5 P.C. Card
	6131	131K	1024x 128	10 μs	10^5	±5,+5,-20	Unknown	-55°C to+125°C	-65°C to+150°C	24 (Hybrid)	2 Years	Unknown	4.5x5.5 P.C. Card
Sperry Univac (Note 5)	50810	8K	256x32	500 μs Write 500 μs Read	Unknown	+12,-18	500MW/ Write	-55°C to+125°C	-55°C to+125°C	16 (Flat Pack)	In Test	Unknown	Pulsed control signal

NOTES:
1. The 2810 is block erase only. GI planning larger and faster N-channel devices, would prefer to sell hybrids rather than dies.
2. The 7451 is presently in the R&D stage. Not planning any larger devices. Will sell dies tested to room temperature and will consider possibility of selling hybridized devices.
3. Parts may be screened to operate from -55° to +125°C (possible but not probable). Will sell dies; not planning larger devices.
4. Will not sell dies and are reluctant to sell basic BORAM device (hybrid units). Westinghouse is working on a smaller package with same pinout arrangements. Also, access time is from stable data to first bit.
5. Will not sell dies but will sell hybrid. Planning a 65K device at the very least, possibly higher.

ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY (E^2PROM's)

E^2PROM's are also solid-state nonvolatile memory devices. Their construction differs from EAROM's in that they use a floating gate MNOS transistor as the data storage element. E^2PROM's have a thicker oxide layer, 200Å versus 25Å for EAROM's, causing stored charge to leak off slower than in the EAROM. The transistor consists of a thin oxide layer separating the P-well from the polysilicon floating gate and a nitride/oxide layer separating the floating gate from the control gate (higher device). Data is stored by causing electrons to tunnel into and out of the floating gate structure. The nitride/oxide sandwich insures strong capacitive coupling between the two gate structures so that lower voltages can be used for erasing and writing.

Motorola has a 2K X 8 device and will be evaluating 4K X 8 E^2PROM in mid-1981. INTEL will be sampling a 2K X 8 device in the next few months. Hughes offers 1K X 8 and 1K X 4 CMOS devices, but both require pulsed power supplies. Hitachi has a 2K X 8 device which also requires a pulsed program voltage. XICOR has a 1K X 1 E^2PROM and is the only company offering a standard Random Access Memory (RAM) array with a shadow E^2PROM section. Ten milliseconds is required for the entire contents of RAM to be programmed into the nonvolatile E^2PROM section. A T^2L signal and 1.5 μs is all that is required to move the E^2PROM contents back into RAM. XICOR will be evaluating 1K X 4 device in 1981.

The largest E^2PROM contains 32K bits and is presently being developed by Motorola. They also offer a 16K device along with INTEL and Hitachi. Hughes presently has an 8K and a 4K CMOS E^2PROM "shadow" area available as a 1K X 1 part. INTEL and Motorola have no plans to develop larger devices.

The Hitachi and both Hughes E^2PROM require power supply packing. All others are static devices.

The INTEL E^2PROM dissipates 500 mw, the highest value of the group. Hitachi is next with 300 mw, and XICOR with 200 mw; the Hughes CMOS devices require the least: 170 mw. Power dissipation figures for the two Motorola devices were not available.

All devices except XICOR's 1K X 1 require two power supplies: +5 VDC and +17 VDC to +25 VDC. The XICOR chip requires only +5 VDC.

Temperature range information was not available for the INTEL chip or the Motorola 32K device. Motorola's 16K chip has an operating range of -10°C to 85°C. A storage temperature range was not available. Both XICOR and Hitachi parts operate at 0-70°C. Only Hughes offers an operating temperature range of -55°C to 125°C. The storage temperature range for the Hughes, XICOR and Hitachi devices is -65°C to 125°C.

Write and erase times for the Motorola 32K and the INTEL E^2PROM were not available. The Hughes CMOS chips are the fastest requiring only 100 μs/8 bits to write and 100 μs to byte or chip erase. XICOR is next taking 10 ms to write the RAM half of memory into the E^2PROM half. Hitachi takes 1 second to erase the entire chip while taking only 800 μs to program 8 bits. The Motorola chip takes 50 ms to chip erase and 10 ms/byte write time. The E^2PROM technology, as of December 1980, is summarized in Table 9.

TABLE 9. E^2 PROM TECHNOLOGY STATUS

VENDOR	PART NUMBER	STORAGE CAPACITY (IN BITS)	DESIGN	ELECTRICAL CHARACTERISTICS				TEMPERATURE CHARACTERISTICS		I/O PINS	AVAIL-ABILITY	COST	INTERFACE COMPLEXITY
				ACCESS TIME	READ/ WRITE CYCLES	VOLTAGES REQUIRED	POWER DIS-SIPATION	OPERATING	STORAGE				
HUGHES (Note 1)	HNUVM 3004	4096	1024x4	200 μs	10^5	+5,+17	170MW, Max	-55°C to +125°C	-65°C to +125°C	24	Off the shelf	$200	Pulsed power supplies
	HNUXM 3008	8192	1024x8	200 μs	10^5	+5,+17	170MW, Max	-55°C to +125°C	-65°C to +125°C	24	Off the shelf	$400	Pulsed power supplies
Motorola (Note 2)	2816	16K	2048x8	Block Erase 850 μs Write 10MS	10^5	Unknown	Unknown	Unknown	Unknown	Un-known	1981 Pro-duction	$25	- - -
	- - -	32K	4096x8	Unknown	10^5	Unknown	Unknown	Unknown	Unknown	Un-known	Sample mid 1981	Un-known	- - -
Intel (Note 3)	2816	16K	2048x8	Unknown	10^4	+5,+20	500MW	Unknown	Unknown	Un-known	Sample 30-60 days	Expen-sive	- - -
XICOR (Note 4)	X2201	1024	1024x1	10MS Array Write	Unknown	+5	200MW	0 to +70°C (Note 5)	-65°C to +125°C	18	Now	$75	- - -
Hitachi (Note 6)	48016	16K	2048x8	1 sec Erase 8 μs Write	10^3 to 10^5	+5,+25	500MW	0 to 70°C	-65°C to +125°C	24	2-3 Weeks	Unknown	Pulsed pro-gram voltage

NOTES:

1. Hughes is willing to sell dies but not temperature tested. Planning larger devices (32K E^2 PROM) for third quarter 1981 plus a 32K EAROM later; both devices are CMOS.
2. Motorola is willing to sell dies tested only at 25°C. Presently looking at mil-temperature devices.
3. Intel is willing to sell dies and are looking for second source. Devices will be single byte erasable.
4. XICOR would prefer to sell hybrid rather than dies. Are considering larger (1K x 4) device in 1981.
5. RAM and recall operates at mil temperature; however, data storage into E^2PROM is a problem at mil temperatures.
6. Hitachi will not sell dies. The device chip erase is compatible with 2716.

SYSTEM DESIGN

GENERAL DESCRIPTION

A total operational Accident Information Retrieval System (AIRS) consists of a helicopter mounted solid-state electronics unit, a Portable Ground Unit (PGU), aircraft mounted sensors, and a ground-based Central Processing Computer facility.

The AIRS flight unit contains the interface electronics to aircraft mounted sensors and an armored module which houses the solid-state, nonvolatile memory device in which recorded aircraft data is stored. The armored module is designed to protect the memory device from the severe environments resulting from aircraft accidents.

The PGU provides a means of recovering data from the AIRS electronics unit when an incident leaves the unit intact and functional. In cases where the electronic unit is destroyed, the memory device can be removed from the wreckage and connected to a functioning AIRS electronics unit for data retrieval. The recovered data is stored on PGU cassette tape and transmitted, by means of the PGU, over telephone lines to a central data processing facility or physically transferred to the facility for input, over an RS232 interface, to the central processing unit. In either case, the cassette can become a permanent record of the incident.

The Central Processing Computer facility is then able to evaluate the aircraft data via ground software for the accident investigation process. The computer facility would process the data and present it in timely fashion in the form of plots and reports to the crash investigation team. The total AIRS concept is shown in block diagram form in Figure 1.

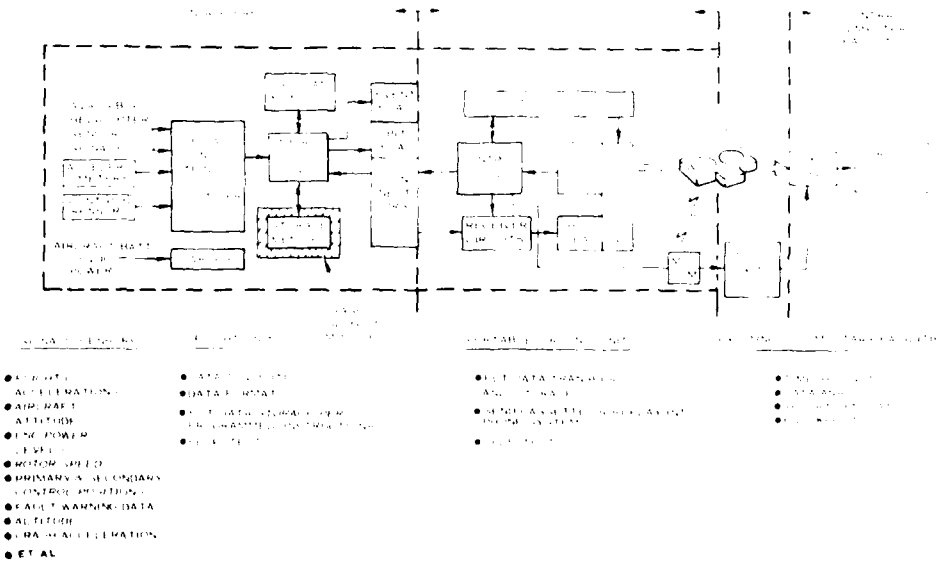


FIGURE 1. BLOCK DIAGRAM - TOTAL AIRS

The AIRS solid-state electronic unit is located in each helicopter to interface with existing or additional aircraft sensors (as required) which provide flight information such as altitude, altitude rate, airspeed, attitudes, engine power condition, control positional indications, acceleration, and fault warning data (see Figure 2).

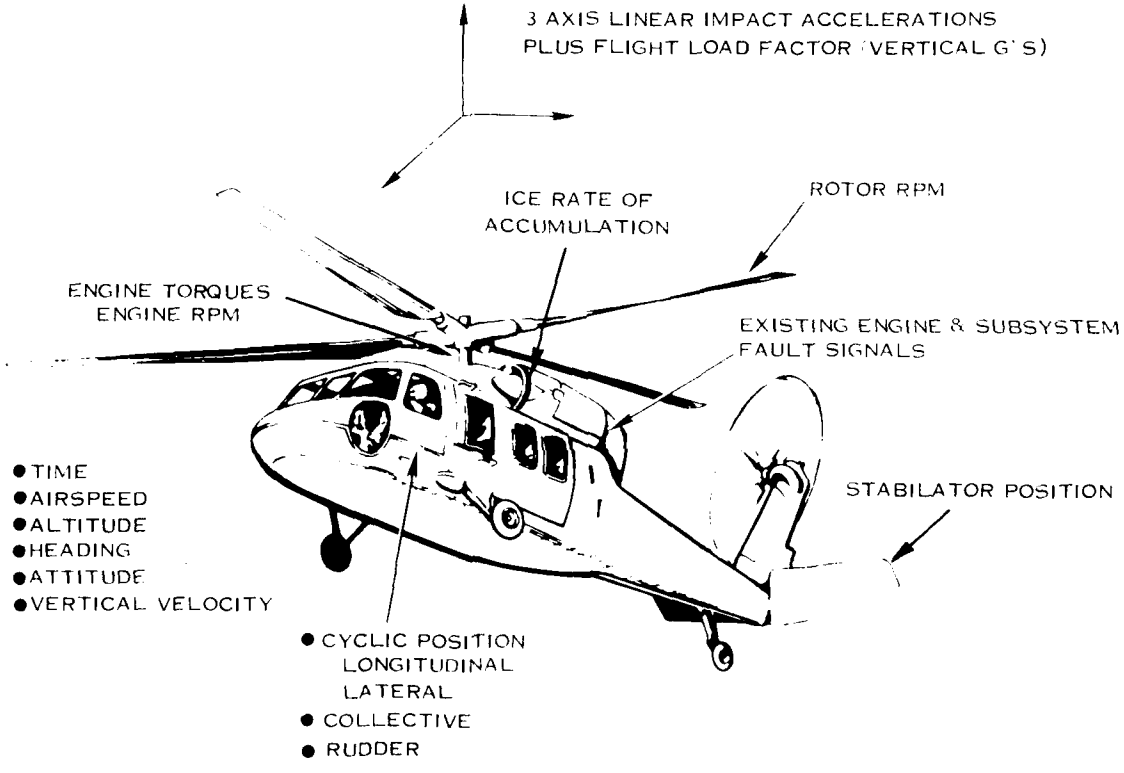


FIGURE 2. BLACK HAWK PARAMETERS RECORDED BY AIRS

Also included are three axes of impact accelerometers. The aircraft parameters are signal conditioned and converted into digital format for storage, under microprocessor control, in the solid-state memory device. The microprocessor performs a selected data storage function by periodically storing data points and updated data values as necessary. The microprocessor operates from rules stored in program memory to selectively store digital data in the solid-state memory device. Precautions are taken in the design of the system to assure that the unit is powered up by the engine start switch(es). The power remains on until the microprocessor shuts itself down following conditions which indicate that the helicopter cannot still be flying. Using the microprocessor, a high level of built-in-test is accomplished. Fault indication is provided and, on more serious faults, the unit is automatically shut down.

AIRS PARAMETERS

The AIRS input parameters are shown in Tables 1 (DC Analogs), 2 (AC Analogs), and 3 (Discretes) for the Sikorsky BLACK HAWK and in Table 4 for the Hughes AAH helicopter. The production configuration for the BLACK HAWK is defined.

The AIRS microprocessor selectively stores data in the CSMM such that a maximum amount of information is stored in a minimum amount of memory in order to keep cost, size, and weight at a minimum. If the parameter is continuous, such as airspeed, a new value plus identification and relative time is stored. Figure 3 illustrates the process. When the last stored value or floating point, plus or minus a limit value, is exceeded a new data point is stored establishing a new floating point value (points 1, 2, 3, 4 and 5 are such points). At fixed periodic intervals of 1 minute, as noted by the double circled points, a reference point in time and value for all parameters is stored in memory. In the production configuration, on-off data will also be similarly stored when a state change takes place.

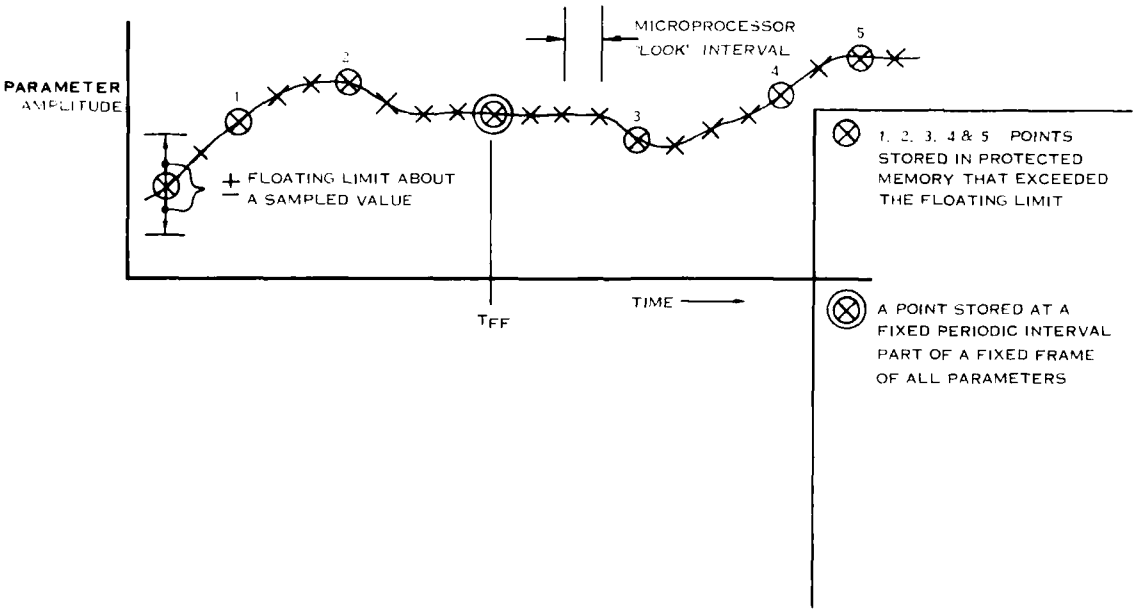


FIGURE 3. AIRS SELECTIVE RECORDING PROCESS

SIGNAL DEFINITIONS

Time

The independent variable for the recorded data is time. It is not necessary to have an absolute time base. Absolute time would add unnecessary expense and operating inconvenience to the system. In virtually every case, it is possible to determine the correlation with absolute time by flight records or the known time of external events. However, it is necessary to know the relative time of the recorded data. This relative time is generated by the operation of the system itself. If data were recorded continuously, the relative time could be determined implicitly by the known recording rate. However, in general, the data will not be recorded continuously and it will be necessary to have a word which uniquely defines the time that each parameter is recorded. The minimum resolution required, except for crash accelerations, is 1 second. The maximum range is dependent on the organization of the data. The interval between reference recordings is 1 minute. Six bits would then be necessary for time resolution between reference recordings for all parameters. Thus, the reference frames are recorded with 1 minute resolution time reference; eight bits will give a total time of 256 minutes or over 4 hours, which is more than adequate to provide unique time reference for all reference frame data. These frames are recorded on the zero second reference time. Data between reference frames is recorded with the elapsed time from the last reference frame. Six bits provides the seconds to cover the time between reference frames.

Airspeed

The AIRS receives airspeed from an airspeed indicator. The production BLACK HAWK helicopter provides a linear airspeed signal with a range of 30 to 180 knots. The recorded resolution will be 3.04 knots with a floating limit of 6.08 knots.

Altitude

The required range of altitude is -1000 to 30,000 feet with 100 foot resolution. This is provided by the reporting altimeter in the form of a digital grey code of 9 bits. The data is saved in the periodic frames and any time a bit in the code changes.

Heading

The heading input into the AIRS is a synchro signal from a directional gyro or gyro compass system. The heading resolution planned is 2 degrees with a range of 360° which requires eight data bits in the stored data. The data is stored to 2-degree resolution in periodic frames and on any changes.

Pitch and Roll Attitude

The AIRS unit requires synchro inputs for pitch and roll from a vertical gyro. These signals are included in the periodic frame and saved upon exceedance of the floating limit criteria. The signal range is ±180° with a resolution of 1

degree which requires 9 bits of data for storage. The data will be included in the periodic frames and on exceedances of the 2-degree floating limit criteria.

Primary Controls

The lateral, longitudinal, collective and pedal control positions are input to the AIRS as DC signals. The signals will be provided from potentiometers installed in the aircraft and the added sensors will be excited from the AIRS unit. The resolution planned is 3.2% of full scale for each signal requiring 5 data bits per signal. The data will be included in the periodic frames and on exceedance of the 6.4% floating limit criteria.

Load Factor

Load factor (vertical flight acceleration) is a DC signal proposed with a range of -1.5 to +3.5g on the production aircraft. The planned resolution for the production aircraft is 0.16g. Limit exceedance will be 0.32g.

Stabilator Position

The stabilator position in the production aircraft is defined by the sum of two stabilator actuator positions or by a synchro. As presently planned, the two actuator positions are to be used for stabilator position; however, since the revision of the input signal capability, it is probable that the stabilator position synchro signal will be used, reducing the spare synchro capacity and freeing up two DC signal channels. The planned resolution using the synchro signal is 3.2% of total stroke with a limit exceedance of 6.4% of total stroke.

Vertical Velocity

Vertical velocity (altitude rate) is a DC signal. The range will be +6000 feet per minute. The resolution planned is 46.8 feet per minute. Limit exceedance will be 93.6 feet per minute.

Ice Rate

The ice rate sensor is an optional piece of equipment on the helicopter and is not available on the flight test helicopter. On the production helicopter, the resolution is planned to be 0.04 gram/cubic meter with a limit exceedance of 0.08 gram/cubic meter.

Engine Torques

The engine torques are provided from the helicopter sensors. The torque range is 0 to 150% with a recording resolution of 2.23% and a limit exceedance of 4.46%

Engine Gas Generator Speed

The engine gas generator speed is provided from the helicopter sensors. The range is 0 to 110% and the recording resolution and limit exceedance are 1.5% and 3% respectively at 100% RPM and 0.38% and 0.76% respectively at 50% RPM.

Rotor Speed

The rotor speed is provided from the helicopter sensors. The range is 0 to 130% with a recording resolution of 2% and a limit exceedance of 4% at 100% RPM.

Discrete Signals

The AIRS will handle 48 discrete signals. One of these is a mode control and is recorded. It selects between the operating program and the ground readout. The remaining discrete inputs will be included in the periodic frames and saved whenever a discrete changes state.

ELECTRONIC DESIGN

The AIRS unit, see Figure 4, incorporates the latest state-of-the-art technology in an all solid-state design providing the advantages of low power dissipation, high reliability, and low weight/volume features. The heart of the AIRS unit is a microprocessor. Resident software programs control and manipulate the flow of aircraft sensor data and selectively store the data in a crash-protected nonvolatile solid-state Electrically Alterable Read Only Memory (EAROM) in the Crash Survivable Memory Module (CSMM).

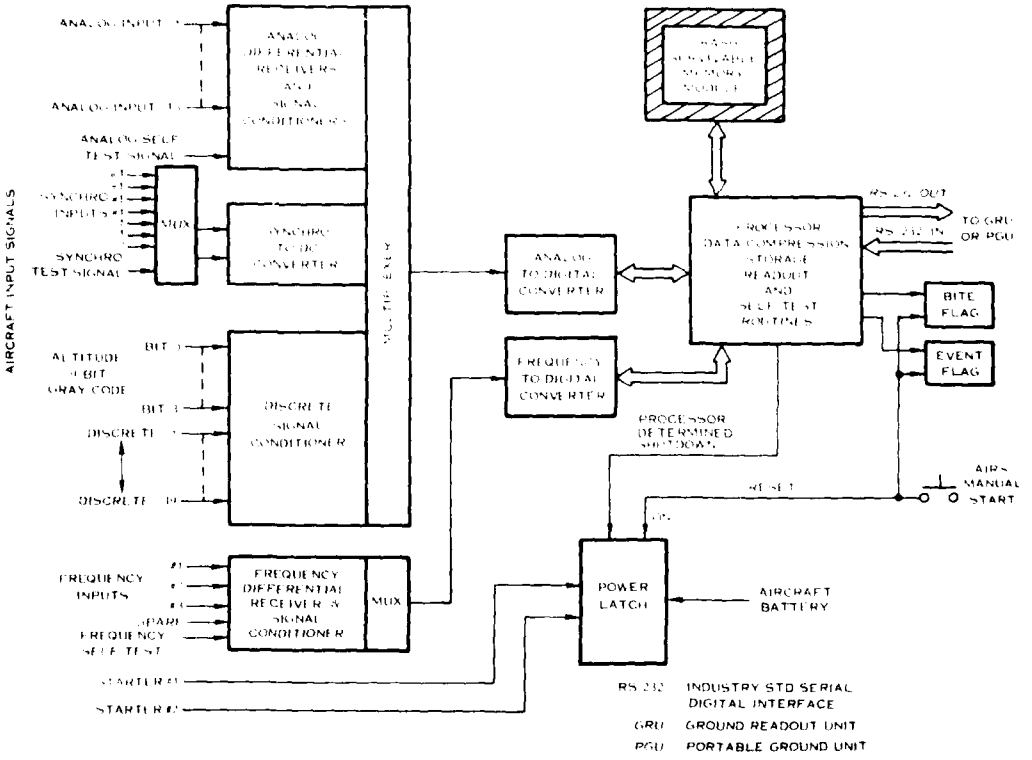


FIGURE 4. AIRS UNIT BLOCK DIAGRAM

The AIRS unit requires direct connection to the aircraft 28V battery bus via a power latch circuit. Power to activate the internal circuitry of the AIRS unit is withheld, to prevent unnecessary drain on the aircraft batteries, until such time that any aircraft engine start switch is activated. The power is then latched to the internal AIRS circuitry and the microprocessor initializes, automatically performs checks on its own operational status to assure proper operation, and proceeds into normal operation.

The data-gathering process, i.e., storing data in the nonvolatile solid-state crash protected memory, is inhibited until such time that engine power is sufficient to provide lift-off. This feature is incorporated in order to avoid the storing away of data which provides no useful information relative to accident investigative procedures. Conversely, as engine power and rotor rpm fall below certain levels for a period of 3 minutes, the microprocessor, under software command, disengages the AIRS power latch and initiates shutdown of the AIRS unit.

The selected shutdown criterion for the AIRS is rotor rpm and at least one engine rpm below 20% for 3 minutes. The production AIRS is designed to withstand impact shocks up to 150g and still retain its data storage input capability dependent upon external retention of battery power cable integrity and also retention of battery input voltage levels. This feature thus allows recording of data related to helicopter motions beyond initial impact.

DC Signal Conditioning

The AIRS is capable of accepting up to 15 differential input DC signals and an internally generated self-test signal. These signal channels provide filtering and attenuation for the full-scale input signal range.

Each channel has a single pole filter with a cutoff frequency suitable for the input signal on that channel, normally 10 Hz. Discrete resistance components are used to provide a high input impedance which will have a minimum loading effect on the input signals. After filtering and attenuation, the DC signals are multiplexed to a differential amplifier with good common mode rejection up to ± 5 VDC or 5 VRMS at 400 Hz.

The 15 differential input DC signals and the self-test signal are individually filtered and attenuated on the basis of either ± 15 volts or ± 10 volts for the full-scale input signal range. Since the A/D converter has 10 bits of output, a part-range input signal, such as zero to +5 volts, will still have 8 bits of resolution.

The A/D converter requires a unipolar input signal. Thus, the ± 5 volt signal level from the differential amplifier is biased up 5 volts to produce a zero to +10 volt signal range to the A/D converter. This bias voltage is derived from the +10 volt A/D reference voltage, and so provides a fixed 50% offset of the converter output.

A block diagram of the AIRS DC analog and discrete signal conditioning circuit is shown in Figure 5.

Discrete Signal Conditioning

The AIRS will accept 48 discretes, received as single ended signals, which have individual low pass filters.

Low voltage (+10V) series discretes, shunt discretes, and high voltage (+28V) series discretes are accommodated. All discretes have a first-order low pass filter with a nominal 30-Hz cutoff frequency.

The discrete signals are multiplexed to the same differential amplifier used for the DC signals. When handling discretes, the amplifier requires a ground reference and the bias voltage must be removed. These are accomplished by two field effect transistor (FET) switches under microprocessor control (see Figure 5).

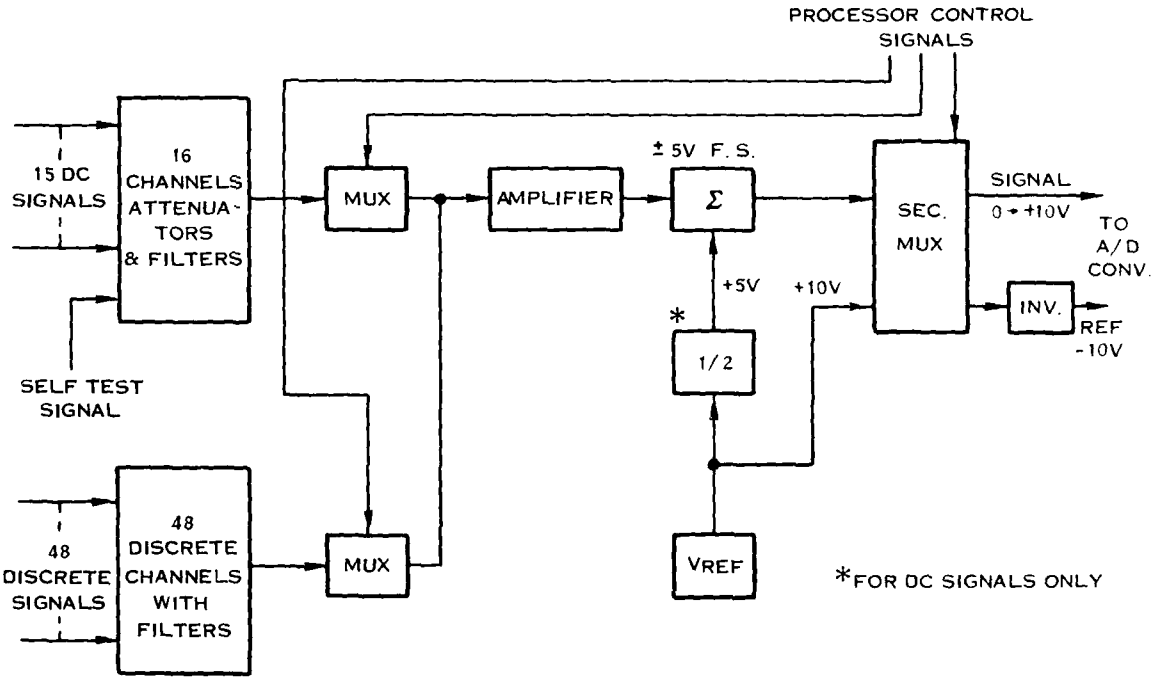


FIGURE 5. AIRS DC AND DISCRETE SIGNAL CONDITIONER

Synchro Signal Conditioning

The AIRS synchro converter will accept three-wire information for up to 7 synchros. A 26-VAC, 400-Hz reference voltage is also required for carrier phase information.

The synchros, along with a test signal, are multiplexed to common conversion circuits. The synchro reference signal for the conversion is selected by processor control based on bus switch discrete input signal.

The conversion approach used requires neither Scott Tee transformation nor division. Referring to the block diagram, see Figure 6, a differential connection of amplifiers is used to form two line-to-line synchro voltages XY and ZY. Comparators generate the signals "C" and "D" when XY and ZY respectively are positive. After XY and ZY are sent through absolute value circuits, another comparator generates the signal "A" when $|XY| > |ZY|$. The gain scaling amplifier of the absolute value circuit is used to provide a 6-Hz filter.

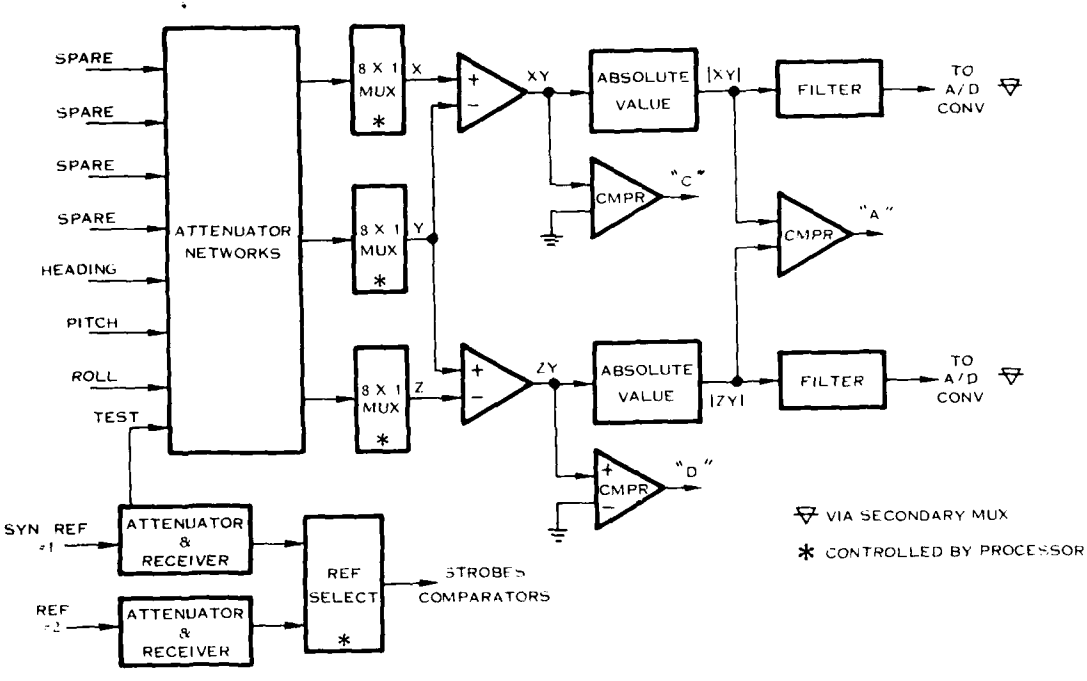


FIGURE 6. BLOCK DIAGRAM - AIRS SYNCHRO CONVERTER

The A/D converter is used to form the ratio of the magnitudes of XY and ZY. The "A" signal is used to select the larger signal as reference for the A/D converter. Thus, for $|XY| > |ZY|$, the "A" signal is 1 and the A/D output, V_R, is:

$$V_R = \frac{|ZY|}{|\overline{XY}|}$$

When $|ZY| > |XY|$, then A = 0, and

$$V_R = \frac{|XY|}{|\overline{ZY}|}$$

Recall that XY and ZY are varying sinusoidally at 400 Hz. Their phase is such that the magnitude of one or the other is always equal to or greater than one-half of the peak magnitude. Thus, the ratioing A/D converter never has a reference smaller than one-half of full scale.

The basic conversion scheme depends on the identifier for the synchro angle given below:

RANGE	OCTANT LOGIC A	C	D	EXPRESSION	V_R SIGN
30^o to 60^o	1	0	1	$= 90 - \text{TAN}^{-1} \frac{1 + 2 V_R}{\sqrt{3}}$	+
60^o to 120^o	1	0	0		-
120^o to 180^o	0	0	0	$= 150 + \text{TAN}^{-1} \frac{1 + 2 V_R}{\sqrt{3}}$	-
180^o to 210^o	0	1	0		+
210^o to 240^o	1	1	0	$= 270 - \text{TAN}^{-1} \frac{1 + 2 V_R}{\sqrt{3}}$	+
240^o to 300^o	1	1	1		-
300^o to 360^o	0	1	1	$= 330 + \text{TAN}^{-1} \frac{1 + 2 V_R}{\sqrt{3}}$	-
360^o to 30^o	0	0	1		+

Note that the TAN^{-1} term is subtracted when A = 1. The sign of $\pm 2 V_R$ is derived from the processing of the C and D voltages through an exclusive "OR" gate. If A, C, D, and V_R are recorded, it is apparent that ground software can reconstruct the synchro angle. A low order of component accuracy is required due to the relatively large percent change of amplitude per degree error.

A synchro test signal also provides verification of the hardware.

Frequency Signal Conditioning

Four frequency signals and a test signal are accepted by the frequency conditioner. The inputs may be sine wave frequencies to high voltage levels, or rectangular pulse signals (see Figure 7).

The differential attenuator and comparator provide good common mode rejection. Comparator hysteresis provides further noise rejection and improves the zero crossing characteristic.

A digital multiplexer feeds all frequency signals to a common programmable interval timer under processor control. It generates a time window lasting 6 periods of the unknown incoming frequency. This window gates a 16-bit counter fed from a high frequency clock. Thus, the count is inversely proportional to the unknown frequency. The use of 6 periods provides an adequate count resolution for the highest incoming frequency, and yet does not allow the counter to overflow except for speeds well below the normal operating range.

A self-test frequency signal verifies both the hardware path and processor control of the interval timer.

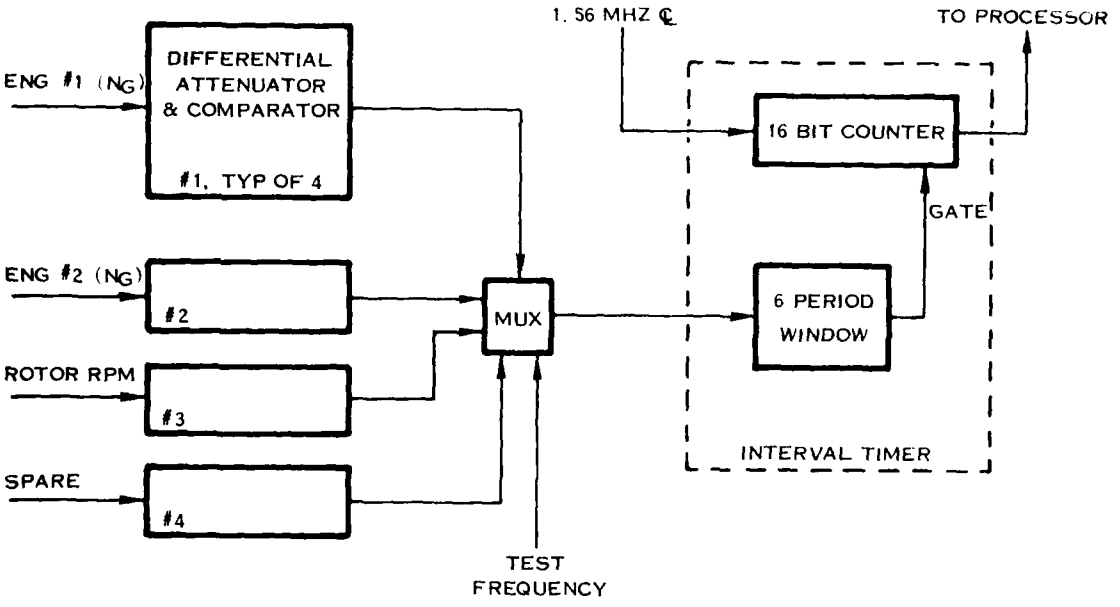


FIGURE 7. BLOCK DIAGRAM - AIRS FREQUENCY CONDITIONER

AIRS Power Supply (see Figure 8)

There are several functions performed by the power supply section.

1. Provide regulated DC voltages.

   a. Internal

      The analog conditioners, the digital processor, and the nonvolatile memory are provided with necessary voltages (5, ±10, ±15, and -20).

   b. External

      Up to eight external signal potentiometers of 5K ohm impedance are supplied with ±10 volts.

2. Provide solid-state power switch.

   a. Accepts a turn-on command from any of the two engine switches or a manual switch.

   b. Turns off power upon command from the microprocessor.

3. Provide power source protection and monitoring.

   a. Protects battery connection against disruptive EMI effects.

   b. Protects against catastrophic component failure by fuse.

   c. Sends a signal to the the microprocessor if input voltage is lost, and provides energy storage for orderly shutdown sequence of non-volatile memory.

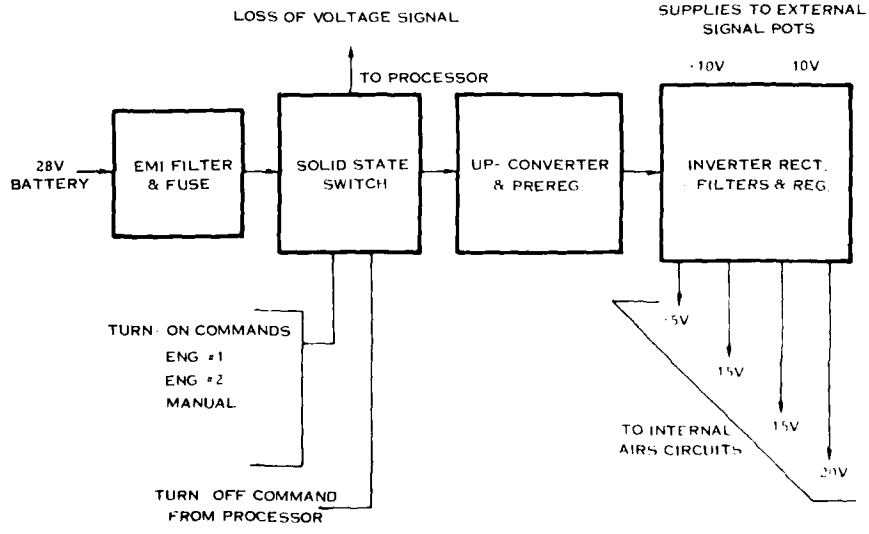


FIGURE 8. BLOCK DIAGRAM - AIRS POWER SUPPLY

An efficient high frequency up-converter provides energy storage at higher than battery voltage, thus reducing required capacitance by the square of the up-conversion ratio. The required up-converter voltage feeds a high frequency inverter.

The input current requirement of the inverter is lowered, due to the high voltage, and the monolithic pulse width modulator (PWM) chip is sufficient to drive the inverter power transistors without an intermediate stage. The inverter power transistors are the small TO-5 type.

The output voltages are derived by rectifying and filtering secondary windings on the inverter transformer. Due to preregulation of the up-converter, relatively fixed loads and high voltage energy storage, the range of pulse width modulation to regulate the output is small. With the inverter running at nearly square waveshape and full wave rectification, the output filter requirements are minimized.

The inverter regulator loop is closed around the +5 volt output. The ±15 volt and -20 volt outputs are changed slightly by transformer and filter load effects but do not require separate regulating loops.

The +10 volt supply has a separate chip regulator, and the -10 volt is derived from the +10 volts via an inverting amplifier and booster transistor.

Analog Multiplexing

Fifteen channels of analog multiplexing are provided which are compatible with the signal conditioner outputs. The multiplexer outputs are digitized by a 10-bit A/D converter which has a maximum conversion time of 20 microseconds. The accuracy of the A/D output signal from the input to the multiplexer is 0.25% of the input signal, including manufacturing tolerances, temperature effects, offsets, and channel cross-talk.

I/O Ports

A two-wire RS232 compatible input and output signal is provided for stored data dump and real time readout of selected input signals. The RS232 input is used for handshaking funtions in data dump/data read back for verification and selection of maintenance readout parameters to be output. The maintenance readout and data dump modes inhibit the normal data storage operation.

Fault/Event Indicators

Magnetic latching indicators are provided to indicate unit failure. The indicator is tripped by microprocessor based software diagnostics or directly by the AIRS watchdog timer. Discrete drive is also provided for remote annunciation to the cockpit caution advisory panel.

The AIRS has been provided with the ability to protect specific data from being overwritten by more recent data until such time that the crash survivable memory data is read out and the protect flags are reset by the ground based PGU. Data surrounding an event such as an in-flight engine shutdown, overtemperature, overstress or exceedance of flight manual limits may be recovered after flight. This arrangement provides a means of preserving data beyond the normal overwrite cycle should the incident occur more than an overwrite cycle time from when the data can be normally retrieved. An output drive and an event latching indicator on the unit similar to the above BIT output are provided. This would assist in incident investigations and aircraft maintenance.

Internal Memory Requirements

A RAM of approximately 1.5K bytes will be available for temporary buffering of data to be written into the crash protected memory device and for scratch-pad usage in the AIRS unit.

Eight thousand (8K) bytes of PROM are available for the AIRS resident operational program which provides adequate room for future expansion.

SOFTWARE DESIGN

Software Routines

The AIRS Software is arranged in three major sections and three interrupt routines (see Figure 9). The three major sections include Initialization, the Normal Background, and the Impact (crash) Acceleration Background. The three interrupt routines are the 2400-Hz interrupt, the frequency interrupt, and the power failure interrupt.

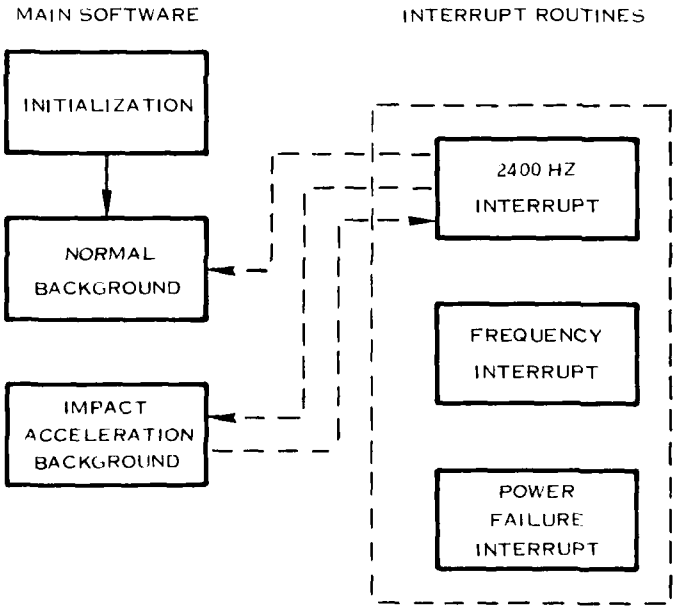


FIGURE 9. AIRS SOFTWARE - GENERAL FLOW

On power up, the program starts with the initialization software (see Figure 10). This section disables the interrupts, initializes all memory, sets up the ports and timers, performs the Built-In-Test (BIT) checks, enables interrupts, and proceeds to the normal background software.

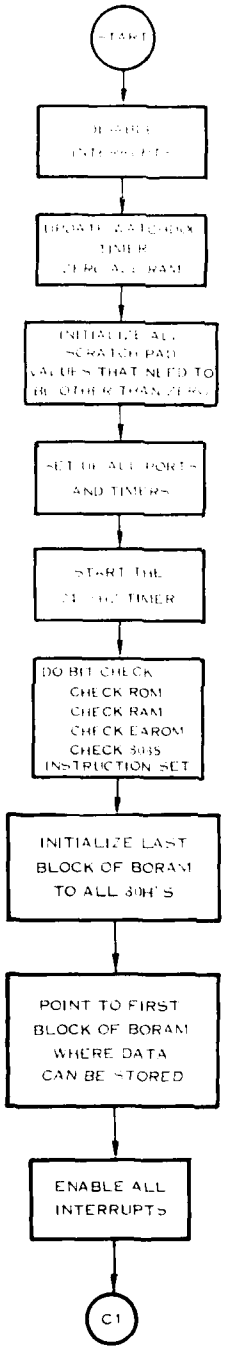


FIGURE 10. AIRS SOFTWARE - INITIALIZATION

The normal background software is actually the main body of the program (see Figure 11). The normal background is a closed 1-second loop that performs all the tests on the parameters, all the periodic BIT checks, all general overhead and timing, and some parameter channel setup. From this closed loop, other functions are interrupt driven.

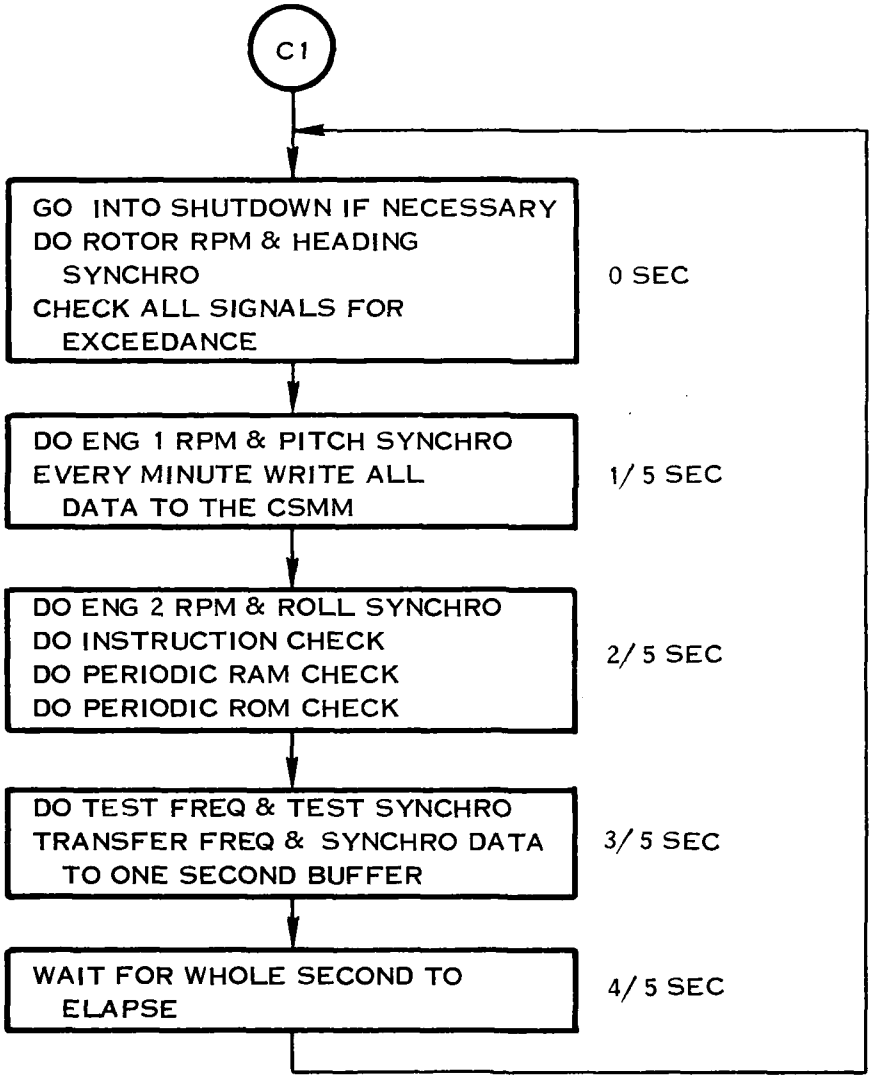


FIGURE 11. AIRS SOFTWARE - NORMAL BACKGROUND

The normal background sets up the frequency and synchro channels because the hardware for these channels takes a longer time to stabilize than the analogs and discretes. The three axes of impact accelerations are all monitored 600 times per second by the 2400-Hz interrupt routines. The remainder of the parameters are handled by the 2400-Hz interrupt routine once a second.

The Acceleration Background software (see Figure 12) is entered from the 2400-Hz interrupt if any of the impact accelerations exceed 7g. The acceleration background will clean up any normal background output that was interrupted and then output acceleration frames until all impact accelerations are below 7g or a maximum number of acceleration frames is reached. The 2400-Hz interrupt will return the program flow to the normal background.

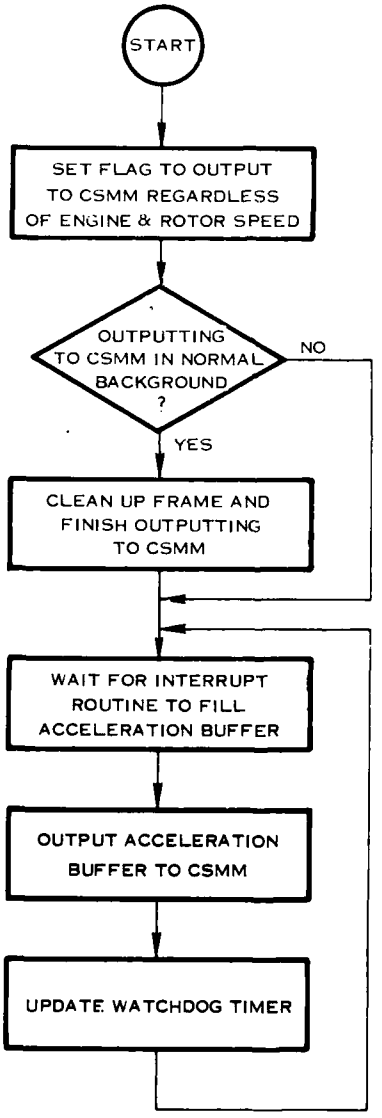


FIGURE 12. AIRS SOFTWARE - ACCELERATION BACKGROUND

The 2400-Hz interrupt routine (see Figure 13) reads and stores the impact accelerations 600 times per second, and the rest of the parameters once a second. The 2400-Hz interrupt routine uses a modulo four cycle to accomplish its function. During one interrupt, the program sets up the A/D for one parameter and reads the parameter that was set up on the previous interrupt. The first three interrupts set up the three impact accelerations and reads the first two. The fourth interrupt reads the last impact acceleration and tests all three accelerations. If any one exceeds 7g, the program exits to the acceleration background. If all are below 7g, the program sets up a list parameter if one is to be done and returns to the normal background software. The fifth interrupt is the modulo 1st, and this sets up the first impact acceleration and reads the list parameter if one was set up. This process is continously repeated during AIRS operation.

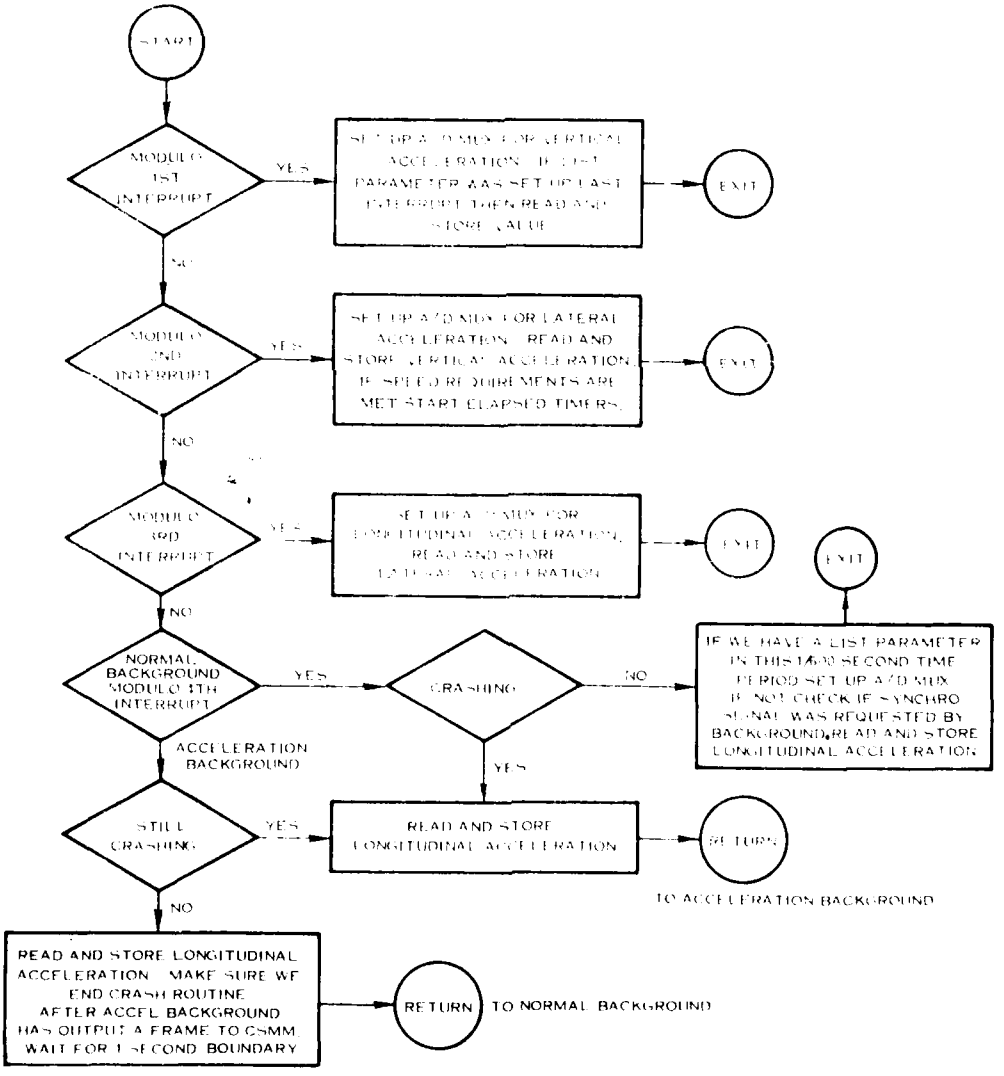


FIGURE 13. AIRS SOFTWARE - 2400 HZ INTERRUPT

The normal background sets up and starts the frequency channels. When the frequency hardware has completed a measurement, the hardware sends an interrupt to the processor. This frequency interrupt (see Figure 14) starts the routine to service the counter. This routine simply tests for an underflow (it's a down counter), reads the counter, and stores the data.

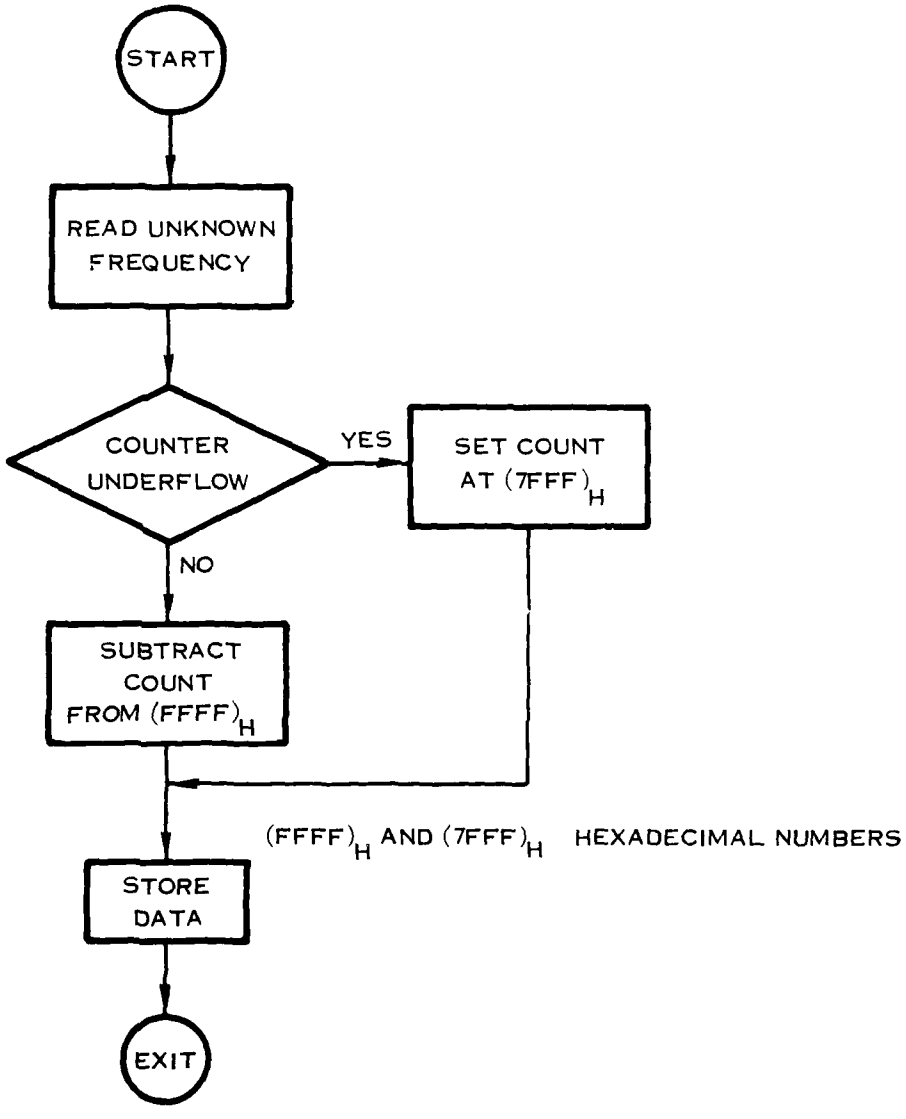


FIGURE 14. AIRS SOFTWARE - FREQUENCY INTERRUPT

The Power Failure Interrupt (see Figure 15) comes when the source power to the AIRS is interrupted. The AIRS power supply has sufficient residual power to allow this routine to output the last data to the solid-state memory device, test for errors, write an error code if necessary, and then go into a loop where the power interruption failure will cause no lost data, i.e., further communication with the memory storage device is inhibited.

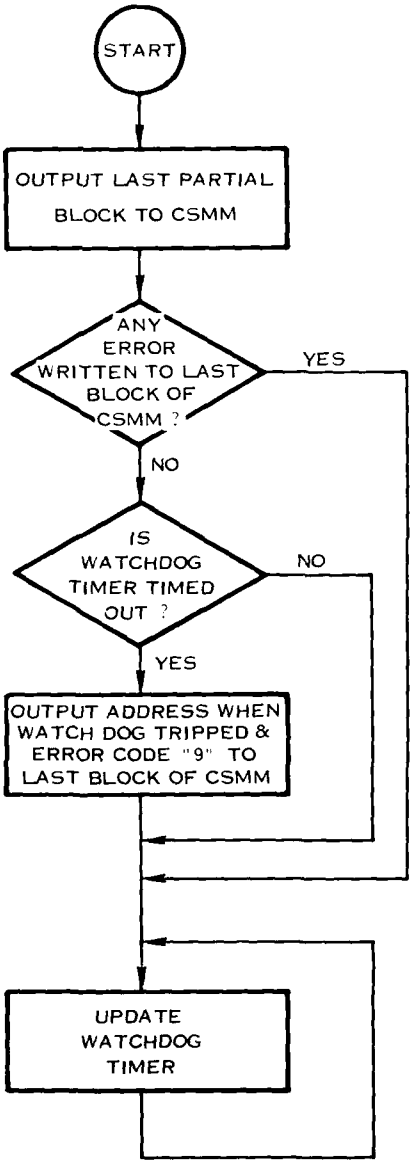


FIGURE 15. AIRS SOFTWARE - POWER FAILURE INTERRUPT

Data Storage

The AIRS data storage in the CSMM has a 32K bit capacity. In the AIRS brassboard, it is a Block Oriented Random Access Memory (BORAM) which is organized into 128 blocks of 256 bits each. Data is written into or read from the data memory one block at a time. Each block is organized as two data frames. The first bit in the frame is a protect bit which when set indicates that the frame is not to be erased and overwritten. If the first bit (bit 0) in a block (first bit in the first frame in the block) is set, the memory system will not allow the block to be erased and overwritten. The next 8 bits (bits 1 through 8) in the frame are a binary minutes count in relative time. The following two bits (bits 9 and 10) are the frame type identification which defines the format and type of data in the remaining bits in the frame. There are four frame types: fixed, mixed, variable, and acceleration.

In the fixed frame, every bit location is defined as a location for a specific parameter bit. The fixed frame is stored once per minute.

The mixed frame is always preceeded by a fixed frame. The mixed frame consists of both location defined data where the bit location is a specific bit in a specific parameter and variable format data where the data defines the structure. The fixed format part of the frame contains the overflow data from the once per minute data sample which would not fit in the fixed frame. Following the fixed format data is a variable format data which is generated by limit exceedances. The variable format data is identified by a 5-bit code which specifies the parameter, followed by 5 bits of binary code which defines the elapsed time since the last fixed frame. This is followed by the parameter data.

The variable frame is used to store limit exceedance data which overflow the mixed frame and has the same variable data format as the variable portion of the mixed frame.

The acceleration frame is fixed data format and handles four sets of data from each of the three crash accelerometer axes.

The CSMM data formats are shown in Tables 10 through 14.

TABLE 10. AIRS SOFTWARE - FIXED FRAME FORMAT

0	128	PROTECT
1	129	MINUTES
2	130	MINUTES
3	131	MINUTES
4	132	MINUTES
5	133	MINUTES
6	134	MINUTES
7	135	MINUTES
8	136	MINUTES
9	137	FRAME TYPE
10	138	FRAME TYPE
11	139	AIRSPEED
12	140	AIRSPEED
13	141	AIRSPEED
14	142	AIRSPEED
15	143	AIRSPEED
16	144	AIRSPEED
17	145	AIRSPEED
18	146	AIRSPEED
19	147	AIRSPEED
20	148	AIRSPEED
21	149	ENGINE #1 TORQUE
22	150	ENGINE #1 TORQUE
23	151	ENGINE #1 TORQUE
24	152	ENGINE #1 TORQUE
25	153	ENGINE #1 TORQUE
26	154	ENGINE #1 TORQUE
27	155	ENGINE #1 TORQUE
28	156	ENGINE #2 TORQUE
29	157	ENGINE #2 TORQUE
30	158	ENGINE #2 TORQUE
31	159	ENGINE #2 TORQUE
32	160	ENGINE #2 TORQUE
33	161	ENGINE #2 TORQUE
34	162	ENGINE #2 TORQUE
35	163	LOADFACTOR
36	164	LOADFACTOR
37	165	LOADFACTOR
38	166	LOADFACTOR
39	167	LOADFACTOR
40	168	LOADFACTOR
41	169	COLLECTIVE STICK
42	170	COLLECTIVE STICK
43	171	COLLECTIVE STICK
44	172	COLLECTIVE STICK
45	173	COLLECTIVE STICK
		BIT 7
		BIT 6
		BIT 5
		BIT 4
		BIT 3
		BIT 2
		BIT 1
		BIT 0
		BIT 8
		BIT 7
		BIT 6
		BIT 5
		BIT 4
		BIT 3
		BIT 2
		BIT 1
		BIT 0
		BIT 8
		BIT 7
		BIT 6
		BIT 5
		BIT 4
		BIT 3
		BIT 2
		BIT 1
		BIT 0
		BIT 8
		BIT 7
		BIT 6
		BIT 5
		BIT 4
46	174	LATERAL STICK
47	175	LATERAL STICK
48	176	LATERAL STICK
49	177	LATERAL STICK
50	178	LATERAL STICK
51	179	LATERAL STICK
52	180	LONGITUDINAL STICK
53	181	LONGITUDINAL STICK
54	182	LONGITUDINAL STICK
55	183	LONGITUDINAL STICK
56	184	LONGITUDINAL STICK
57	185	LONGITUDINAL STICK
58	186	PEDAL
59	187	PEDAL
60	188	PEDAL
61	189	PEDAL
62	190	PEDAL
63	191	PEDAL
64	192	STABILATOR ACTUATOR #1
65	193	STABILATOR ACTUATOR #1
66	194	STABILATOR ACTUATOR #1
67	195	STABILATOR ACTUATOR #1
68	196	STABILATOR ACTUATOR #1
69	197	STABILATOR ACTUATOR #1
70	198	STABILATOR ACTUATOR #2
71	199	STABILATOR ACTUATOR #2
72	200	STABILATOR ACTUATOR #2
73	201	STABILATOR ACTUATOR #2
74	202	STABILATOR ACTUATOR #2
75	203	STABILATOR ACTUATOR #2
76	204	ALTITUDE RATE
77	205	ALTITUDE RATE
78	206	ALTITUDE RATE
79	207	ALTITUDE RATE
80	208	ALTITUDE RATE
81	209	ALTITUDE RATE
82	210	ALTITUDE RATE
83	211	ALTITUDE RATE
84	212	ICE RATE
85	213	ICE RATE
86	214	ICE RATE
87	215	ICE RATE
88	216	ICE RATE
		BIT 8
		BIT 7
		BIT 6
		BIT 5
		BIT 4
		BIT 3
89	217	MOTOR RPM
90	218	MOTOR RPM
91	219	MOTOR RPM
92	220	MOTOR RPM
93	221	MOTOR RPM
94	222	MOTOR RPM
95	223	MOTOR RPM
96	224	MOTOR RPM
97	225	ENGINE #1 RPM (NG)
98	226	ENGINE #1 RPM (NG)
99	227	ENGINE #1 RPM (NG)
100	228	ENGINE #1 RPM (NG)
101	229	ENGINE #1 RPM (NG)
102	230	ENGINE #1 RPM (NG)
103	231	ENGINE #1 RPM (NG)
104	232	ENGINE #1 RPM (NG)
105	233	ENGINE #2 RPM (NG)
106	234	ENGINE #2 RPM (NG)
107	235	ENGINE #2 RPM (NG)
108	236	ENGINE #2 RPM (NG)
109	237	ENGINE #2 RPM (NG)
110	238	ENGINE #2 RPM (NG)
111	239	ENGINE #2 RPM (NG)
112	240	ENGINE #2 RPM (NG)
113	241	HEADING OCTANT
114	242	HEADING OCTANT
115	243	HEADING OCTANT
116	244	HEADING DATA
117	245	HEADING DATA
118	246	HEADING DATA
119	247	HEADING DATA
120		HEADING DATA
121		ROLL OCTANT
122		ROLL OCTANT
123		ROLL OCTANT
124		ROLL DATA
125		ROLL DATA
126		ROLL DATA
127		ROLL DATA
248		CHECKSUM
249		CHECKSUM
250		CHECKSUM
251		CHECKSUM
252		CHECKSUM
253		CHECKSUM
254		CHECKSUM
255		CHECKSUM
		BIT 11
		BIT 10
		BIT 9
		BIT 8
		BIT 7
		BIT 6
		BIT 5
		BIT 4
		BIT 13
		BIT 12
		BIT 11
		BIT 10
		BIT 9
		BIT 8
		BIT 7
		BIT 6
		BIT 5
		BIT 4
		BIT 3
		BIT 2
		BIT 1
		BIT 0
		BIT 13
		BIT 12
		BIT 11
		BIT 10
		BIT 9
		BIT 8
		BIT 7
		BIT 6
		BIT A
		BIT C
		BIT D
		BIT 9
		BIT 8
		BIT 7
		BIT A
		BIT 5
		BIT B
		BIT C
		BIT D
		BIT 9
		BIT 8
		BIT 7
		BIT A
		BIT 5
		BIT B
		BIT 6
		BIT 5
		BIT 4
		BIT 3
		BIT 2
		BIT 1
		BIT 0

TABLE 11. AIRS SOFTWARE - MIXED FRAME FORMAT

0	128	PROTECT	
1	129	MINUTES	BIT 7
2	130	MINUTES	BIT 6
3	131	MINUTES	BIT 5
4	132	MINUTES	BIT 4
5	133	MINUTES	BIT 3
6	134	MINUTES	BIT 2
7	135	MINUTES	BIT 1
8	136	MINUTES	BIT 0
9	137	FRAME TYPE	0
10	138	FRAME TYPE	1
11		HEADING DATA	BIT 5
12		ROLL OCTANT	BIT A
13		ROLL OCTANT	BIT C
14		ROLL OCTANT	BIT E
15		ROLL DATA	BIT 9
16		ROLL DATA	BIT B
17		ROLL DATA	BIT D
18		ROLL DATA	BIT F
19	139	ROLL DATA	BIT 5
20	140	ROLL DATA	BIT 4
21	141	PITCH OCTANT	BIT A
22	142	PITCH OCTANT	BIT C
23	143	PITCH OCTANT	BIT E
24	144	PITCH DATA	BIT 9
25	145	PITCH DATA	BIT B
26	146	PITCH DATA	BIT D
27	147	PITCH DATA	BIT F
28	148	PITCH DATA	BIT 4
29	149	ALTITUDE	BIT 8
30	150	ALTITUDE	BIT 7
31	151	ALTITUDE	BIT 6
32	152	ALTITUDE	BIT 5
33	153	ALTITUDE	BIT 4
34	154	ALTITUDE	BIT 3
35	155	ALTITUDE	BIT 2
36	156	ALTITUDE	BIT 1
37	157	ALTITUDE	BIT 0
38	158	SAS ARMING	
39	159	SAS/FPS FAIL	
40	160	FIRE DETECTION	
41	161	CHIP DETECTION ENG 1	
42	162	CHIP DETECTION ENG 2	
43	163	HYDRAULIC PRESURE ENG 1	
44	164	HYDRAULIC PRESURE ENG 2	
45	165	HYDRAULIC PRESURE APU	
46	166	SPARE 1	
47	167	SPARE 2	
48	168	VARIABLE FORMAT DATA	
49	169	VARIABLE FORMAT DATA	
50	170	VARIABLE FORMAT DATA	
51	171	VARIABLE FORMAT DATA	
52	172	VARIABLE FORMAT DATA	
53	173	VARIABLE FORMAT DATA	
54	174	VARIABLE FORMAT DATA	
55	175	VARIABLE FORMAT DATA	
56	176	VARIABLE FORMAT DATA	
57	177	VARIABLE FORMAT DATA	
58	178	VARIABLE FORMAT DATA	
59	179	VARIABLE FORMAT DATA	
60	180	VARIABLE FORMAT DATA	
61	181	VARIABLE FORMAT DATA	
62	182	VARIABLE FORMAT DATA	
63	183	VARIABLE FORMAT DATA	
64	184	VARIABLE FORMAT DATA	
65	185	VARIABLE FORMAT DATA	
66	186	VARIABLE FORMAT DATA	
67	187	VARIABLE FORMAT DATA	
68	188	VARIABLE FORMAT DATA	
69	189	VARIABLE FORMAT DATA	
70	190	VARIABLE FORMAT DATA	
71	191	VARIABLE FORMAT DATA	
72	192	VARIABLE FORMAT DATA	
73	193	VARIABLE FORMAT DATA	
74	194	VARIABLE FORMAT DATA	
75	195	VARIABLE FORMAT DATA	
76	196	VARIABLE FORMAT DATA	
77	197	VARIABLE FORMAT DATA	
78	198	VARIABLE FORMAT DATA	
79	199	VARIABLE FORMAT DATA	
80	200	VARIABLE FORMAT DATA	
81	201	VARIABLE FORMAT DATA	
82	202	VARIABLE FORMAT DATA	
83	203	VARIABLE FORMAT DATA	
84	204	VARIABLE FORMAT DATA	
85	205	VARIABLE FORMAT DATA	
86	206	VARIABLE FORMAT DATA	
87	207	VARIABLE FORMAT DATA	
88	208	VARIABLE FORMAT DATA	
89	209	VARIABLE FORMAT DATA	
90	210	VARIABLE FORMAT DATA	
91	211	VARIABLE FORMAT DATA	
92	212	VARIABLE FORMAT DATA	
93	213	VARIABLE FORMAT DATA	
94	214	VARIABLE FORMAT DATA	
95	215	VARIABLE FORMAT DATA	
96	216	VARIABLE FORMAT DATA	
97	217	VARIABLE FORMAT DATA	
98	218	VARIABLE FORMAT DATA	
99	219	VARIABLE FORMAT DATA	
100	220	VARIABLE FORMAT DATA	
101	221	VARIABLE FORMAT DATA	
102	222	VARIABLE FORMAT DATA	
103	223	VARIABLE FORMAT DATA	
104	224	VARIABLE FORMAT DATA	
105	225	VARIABLE FORMAT DATA	
106	226	VARIABLE FORMAT DATA	
107	227	VARIABLE FORMAT DATA	
108	228	VARIABLE FORMAT DATA	
109	229	VARIABLE FORMAT DATA	
110	230	VARIABLE FORMAT DATA	
111	231	VARIABLE FORMAT DATA	
112	232	VARIABLE FORMAT DATA	
113	233	VARIABLE FORMAT DATA	
114	234	VARIABLE FORMAT DATA	
115	235	VARIABLE FORMAT DATA	
116	236	VARIABLE FORMAT DATA	
117	237	VARIABLE FORMAT DATA	
118	238	VARIABLE FORMAT DATA	
119	239	VARIABLE FORMAT DATA	
120	240	VARIABLE FORMAT DATA	
121	241	VARIABLE FORMAT DATA	
122	242	VARIABLE FORMAT DATA	
123	243	VARIABLE FORMAT DATA	
124	244	VARIABLE FORMAT DATA	
125	245	VARIABLE FORMAT DATA	
126	246	VARIABLE FORMAT DATA	
127	247	VARIABLE FORMAT DATA	
248		CHECKSUM	BIT 7
249		CHECKSUM	BIT 6
250		CHECKSUM	BIT 5
251		CHECKSUM	BIT 4
252		CHECKSUM	BIT 3
253		CHECKSUM	BIT 2
254		CHECKSUM	BIT 1
255		CHECKSUM	BIT 0

TABLE 12. AIRS SOFTWARE - VARIABLE DATA FORMAT

N	SIGNAL IDENTIFICATION	BIT 5
N + 1	SIGNAL IDENTIFICATION	BIT 4
N + 2	SIGNAL IDENTIFICATION	BIT 3
N + 3	SIGNAL IDENTIFICATION	BIT 2
N + 4	SIGNAL IDENTIFICATION	BIT 1
N + 5	SIGNAL IDENTIFICATION	BIT 0
N + 6	SECONDS	BIT 5
N + 7	SECONDS	BIT 4
N + 8	SECONDS	BIT 3
N + 9	SECONDS	BIT 2
N + 10	SECONDS	BIT 1
N + 11	SECONDS	BIT 0
N + 12	DATA	MSB

ADDITIONAL LINES AS REQUIRED FOR REMAINING DATA BITS

SIGNAL TABLE

SIGNAL	NUMBER OF BITS	DATA BITS	RESOLUTION
AIRSPEED	BITS 10	0 THRU 9	3.04KTS
ENGINE #1 TORQUE	BITS 7	2 THRU 8	2.23 %
ENGINE #2 TORQUE	BITS 7	2 THRU 8	2.23 %
LOADFACTOR	BITS 6	4 THRU 9	0.16 G'S
COLLECTIVE STICK	BITS 5	4 THRU 8	3.2 %
LATERAL STICK	BITS 6	3 THRU 8	1.6 %
LONGITUDINAL STICK	BITS 6	3 THRU 8	1.6 %
PEDAL	BITS 6	3 THRU 8	1.6 %
STABILATOR ACTUATOR #1	BITS 6	4 THRU 9	1.6 %
STABILATOR ACTUATOR #2	BITS 6	4 THRU 9	1.6 %
ALTITUDE RATE	BITS 8	2 THRU 9	46.8 FPM
ICE RATE	BITS 5	3 THRU 7	0.04 GM./CU. METER
ROTOR RPM	BITS 8	4 THRU 11	2% @ 100% RPM
ENGINE #1 RPM (NG)	BITS 8	6 THRU 13	0.38% @ 50% RPM
ENGINE #2 RPM (NG)	BITS 8	6 THRU 13	1.5% @ 100% RPM
HEADING DATA	BITS 8	5 THRU 12	2 DEG.
ROLL DATA	BITS 9	4 THRU 12	1 DEG.
PITCH DATA	BITS 9	4 THRU 12	1 DEG
ALTITUDE	BITS 9	0 THRU 8	100 FEET
SAS WARNING	BITS 1		DISCRETE
SAS/FPS FAULT	BITS 1		DISCRETE
FIRE DETECTION	BITS 1		DISCRETE
CHIP DETECTION ENG 1	BITS 1		DISCRETE
CHIP DETECTION ENG 2	BITS 1		DISCRETE
HYDRAULIC PRESURE ENG 1	BITS 1		DISCRETE
HYDRAULIC PRESURE ENG 2	BITS 1		DISCRETE
HYDRAULIC PRESURE APU	BITS 1		DISCRETE
SPARE 1	BITS 1		DISCRETE
SPARE 2	BITS 1		DISCRETE
VERTICAL G'S	BITS 8	2 THRU 9	2.4 G'S
LATERAL G'S	BITS 8	2 THRU 9	2.4 G'S
LONGITUDINAL G'S	BITS 8	2 THRU 9	2.4 G'S

TABLE 13. AIRS SOFTWARE - VARIABLE FRAME FORMAT

0	128	PROTECT	
1	129	MINUTES	BIT 7
2	130	MINUTES	BIT 6
3	131	MINUTES	BIT 5
4	132	MINUTES	BIT 4
5	133	MINUTES	BIT 3
6	134	MINUTES	BIT 2
7	135	MINUTES	BIT 1
8	136	MINUTES	BIT 0
9	137	FRAME TYPE	1
10	138	FRAME TYPE	0
11	139	VARIABLE FORMAT DATA	
12	140	VARIABLE FORMAT DATA	
13	141	VARIABLE FORMAT DATA	
14	142	VARIABLE FORMAT DATA	
15	143	VARIABLE FORMAT DATA	
16	144	VARIABLE FORMAT DATA	
17	145	VARIABLE FORMAT DATA	
18	146	VARIABLE FORMAT DATA	
19	147	VARIABLE FORMAT DATA	
20	148	VARIABLE FORMAT DATA	
21	149	VARIABLE FORMAT DATA	
22	150	VARIABLE FORMAT DATA	
23	151	VARIABLE FORMAT DATA	
24	152	VARIABLE FORMAT DATA	
25	153	VARIABLE FORMAT DATA	
26	154	VARIABLE FORMAT DATA	
27	155	VARIABLE FORMAT DATA	
28	156	VARIABLE FORMAT DATA	
•	•	• • •	
•	•	• • •	
•	•	• • •	
114	242	VARIABLE FORMAT DATA	
115	243	VARIABLE FORMAT DATA	
116	244	VARIABLE FORMAT DATA	
117	245	VARIABLE FORMAT DATA	
118	246	VARIABLE FORMAT DATA	
119	247	VARIABLE FORMAT DATA	
120		VARIABLE FORMAT DATA	
121		VARIABLE FORMAT DATA	
122		VARIABLE FORMAT DATA	
123		VARIABLE FORMAT DATA	
124		VARIABLE FORMAT DATA	
125		VARIABLE FORMAT DATA	
126		VARIABLE FORMAT DATA	
127		VARIABLE FORMAT DATA	
248		CHECKSUM	BIT 7
249		CHECKSUM	BIT 6
250		CHECKSUM	BIT 5
251		CHECKSUM	BIT 4
252		CHECKSUM	BIT 3
253		CHECKSUM	BIT 2
254		CHECKSUM	BIT 1
255		CHECKSUM	BIT 0

TABLE 14. AIRS SOFTWARE - ACCELERATION FRAME FORMAT

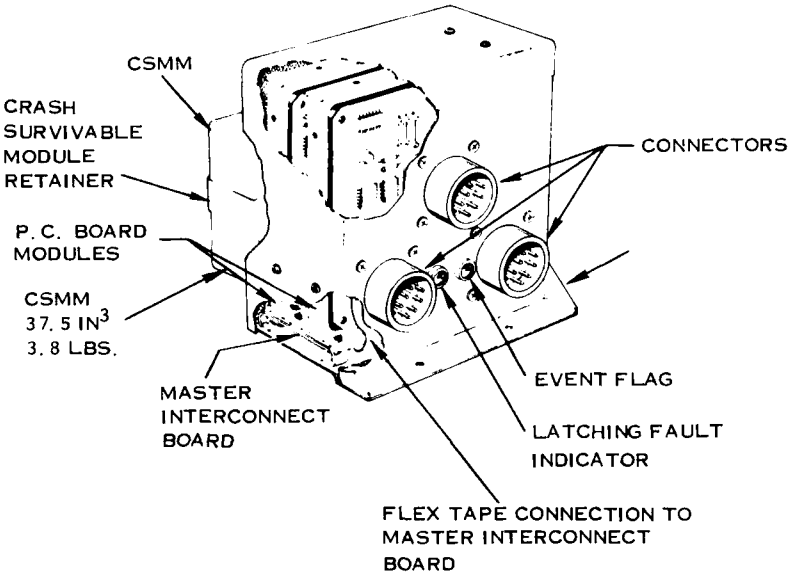
0	128	PROTECT		48	176	VERTICAL G'S	BIT 9	96	224	VERTICAL G'S	BIT 9
1	129	MINUTES	BIT 7	49	177	VERTICAL G'S	BIT 8	97	225	VERTICAL G'S	BIT 8
2	130	MINUTES	BIT 6	50	178	VERTICAL G'S	BIT 7	98	226	VERTICAL G'S	BIT 7
3	131	MINUTES	BIT 5	51	179	VERTICAL G'S	BIT 6	99	227	VERTICAL G'S	BIT 6
4	132	MINUTES	BIT 4	52	180	VERTICAL G'S	BIT 5	100	228	VERTICAL G'S	BIT 5
5	133	MINUTES	BIT 3	53	181	VERTICAL G'S	BIT 4	101	229	VERTICAL G'S	BIT 4
6	134	MINUTES	BIT 2	54	182	VERTICAL G'S	BIT 3	102	230	VERTICAL G'S	BIT 3
7	135	MINUTES	BIT 1	55	183	VERTICAL G'S	BIT 2	103	231	VERTICAL G'S	BIT 2
8	136	MINUTES	BIT 0	56	184	LATERAL G'S	BIT 9	104	232	LATERAL G'S	BIT 9
9	137	FRAME TYPE	1	57	185	LATERAL G'S	BIT 8	105	233	LATERAL G'S	BIT 8
10	138	FRAME TYPE	1	58	186	LATERAL G'S	BIT 7	106	234	LATERAL G'S	BIT 7
11	139	SECONDS	BIT 5	59	187	LATERAL G'S	BIT 6	107	235	LATERAL G'S	BIT 6
12	140	SECONDS	BIT 4	60	188	LATERAL G'S	BIT 5	108	236	LATERAL G'S	BIT 5
13	141	SECONDS	BIT 3	61	189	LATERAL G'S	BIT 4	109	237	LATERAL G'S	BIT 4
14	142	SECONDS	BIT 2	62	190	LATERAL G'S	BIT 3	110	238	LATERAL G'S	BIT 3
15	143	SECONDS	BIT 1	63	191	LATERAL G'S	BIT 2	111	239	LATERAL G'S	BIT 2
16	144	SECONDS	BIT 0	64	192	LONGITUDINAL G'S	BIT 9	112	240	LONGITUDINAL G'S	BIT 9
17	145	SECONDS/100	BIT 6	65	193	LONGITUDINAL G'S	BIT 8	113	241	LONGITUDINAL G'S	BIT 8
18	146	SECONDS/100	BIT 5	66	194	LONGITUDINAL G'S	BIT 7	114	242	LONGITUDINAL G'S	BIT 7
19	147	SECONDS/100	BIT 4	67	195	LONGITUDINAL G'S	BIT 6	115	243	LONGITUDINAL G'S	BIT 6
20	148	SECONDS/100	BIT 3	68	196	LONGITUDINAL G'S	BIT 5	116	244	LONGITUDINAL G'S	BIT 5
21	149	SECONDS/100	BIT 2	69	197	LONGITUDINAL G'S	BIT 4	117	245	LONGITUDINAL G'S	BIT 4
22	150	SECONDS/100	BIT 1	70	198	LONGITUDINAL G'S	BIT 3	118	246	LONGITUDINAL G'S	BIT 3
23	151	SECONDS/100	BIT 0	71	199	LONGITUDINAL G'S	BIT 2	119	247	LONGITUDINAL G'S	BIT 2
24	152	VERTICAL G'S	BIT 9	72	200	VERTICAL G'S	BIT 9	120		SPARE	
25	153	VERTICAL G'S	BIT 8	73	201	VERTICAL G'S	BIT 8	121		SPARE	
26	154	VERTICAL G'S	BIT 7	74	202	VERTICAL G'S	BIT 7	122		SPARE	
27	155	VERTICAL G'S	BIT 6	75	203	VERTICAL G'S	BIT 6	123		SPARE	
28	156	VERTICAL G'S	BIT 5	76	204	VERTICAL G'S	BIT 5	124		SPARE	
29	157	VERTICAL G'S	BIT 4	77	205	VERTICAL G'S	BIT 4	125		SPARE	
30	158	VERTICAL G'S	BIT 3	78	206	VERTICAL G'S	BIT 3	126		SPARE	
31	159	VERTICAL G'S	BIT 2	79	207	VERTICAL G'S	BIT 2	127		SPARE	
32	160	LATERAL G'S	BIT 9	80	208	LATERAL G'S	BIT 9	248		CHECKSUM	BIT 7
33	161	LATERAL G'S	BIT 8	81	209	LATERAL G'S	BIT 8	249		CHECKSUM	BIT 6
34	162	LATERAL G'S	BIT 7	82	210	LATERAL G'S	BIT 7	250		CHECKSUM	BIT 5
35	163	LATERAL G'S	BIT 6	83	211	LATERAL G'S	BIT 6	251		CHECKSUM	BIT 4
36	164	LATERAL G'S	BIT 5	84	212	LATERAL G'S	BIT 5	252		CHECKSUM	BIT 3
37	165	LATERAL G'S	BIT 4	85	213	LATERAL G'S	BIT 4	253		CHECKSUM	BIT 2
38	166	LATERAL G'S	BIT 3	86	214	LATERAL G'S	BIT 3	254		CHECKSUM	BIT 1
39	167	LATERAL G'S	BIT 2	87	215	LATERAL G'S	BIT 2	255		CHECKSUM	BIT 0
40	168	LONGITUDINAL G'S	BIT 9	88	216	LONGITUDINAL G'S	BIT 9				
41	169	LONGITUDINAL G'S	BIT 8	89	217	LONGITUDINAL G'S	BIT 8				
42	170	LONGITUDINAL G'S	BIT 7	90	218	LONGITUDINAL G'S	BIT 7				
43	171	LONGITUDINAL G'S	BIT 6	91	219	LONGITUDINAL G'S	BIT 6				
44	172	LONGITUDINAL G'S	BIT 5	92	220	LONGITUDINAL G'S	BIT 5				
45	173	LONGITUDINAL G'S	BIT 4	93	221	LONGITUDINAL G'S	BIT 4				
46	174	LONGITUDINAL G'S	BIT 3	94	222	LONGITUDINAL G'S	BIT 3				
47	175	LONGITUDINAL G'S	BIT 2	95	223	LONGITUDINAL G'S	BIT 2				

MECHANICAL DESIGN

General

The AIRS mechanical design is comprised of two main subsystems. The electronics unit contains aircraft interface circuitry, signal conditioners, multiplex circuitry, analog-to-digital conversion circuits, the micropocessor control, and resident program memory. The second subsystem consists of the Crash Survivable Memory Module (CSMM) which houses the solid-state nonvolatile memory device.

The design configuration of the AIRS electronics unit for production is shown in Figure 16. The electronic unit is designed to meet the environmental requirements for Class I airborne equipment per MIL-STD-810B. In addition, the AIRS unit will be capable of withstanding 150g, 10-millisecond crash impact shocks while maintaining data recording/storage capabilities for up to 10 seconds beyond initial impact, dependent upon integrity of the interface connections with the aircraft 28 VDC battery bus.



ESTIMATED PRODUCTION CHARACTERISTICS	
● WT. 9.23 LBS. (MAX. EXCL. FLANGES)	
● SIZE 6.5 LONG	
6.5 HIGH	
6.8 WIDE	
● VOLUME 207 IN3	
● MATURE RELIABILITY	10,300 HOURS MTBF
● POWER CONSUMPTION	25 WATTS MAX (15 WATTS AV.) AT 28 VDC

FIGURE 16. AIRS PACKAGE CONCEPT

Production Electronics Unit

The production system is currently estimated to be less than 7 inches cubed and to weigh less than 9.3 pounds including the CSMM. The electronics unit will contain four printed circuit (PC) boards partitioned as follows:

1. Power Supply
2. Analog Signal Conditioner
3. Processor and Frequency Interface
4. Memory Module Control

Each board will measure approximately 5.75 inches X 6.25 inches and will contain eight layers. The four PC boards will be interconnected via a multilayer master interconnect board which will also connect to the AIRS input/output (I/O) connectors and CSMM via flex tapes. I/O connectors will contain sufficient connection for approximately 120 aircraft signal and power lines and sufficient connections for system test and/or data retrieval via a Portable Ground Unit.

An EVENT and BIT latching indicator will be provided for maintenance crew visual inspection to determine system operational status. The EVENT indicator will alert the ground crew that data representing an aircraft unusual incident or response was saved for ground evaluation. Readout of the AIRS memory would then be accomplished with the PGU in order to evaluate the incident. The BIT indicator alerts the ground crew that the AIRS was shut down due to a malfunction and thus requires ground checkout. The BIT indication may indicate either a malfunction of the AIRS or a related sensor malfunction.

The AIRS Electronics Unit housing will be hard-mounted on board the aircraft and will contain open ventilation for convection cooling of the electronics.

The CSMM will be strap mounted to the electronics unit utilizing a burn-away harness which will allow the CSMM to fall away from the electronics during a fire. This design feature is necessary to allow unrestricted intumescing of the CSMM outer insulating shell during a post crash fire.

Crash Survivable Memory Module (CSMM)

The heart of the AIRS is the armored module used to protect the solid-state memory device during and after an aircraft incident involving high impact shocks, piercing loads resulting from aircraft breakup, crushing loads resulting from aircraft wreckage landing on the armored module, flames resulting from ignition of aircraft fuel, and possible submergence in sea water. To accomplish the necessary protection of the memory device, the armored module incorporates four major design features: an intumescent outer shell, an

armored housing, four discrete water-filled insulation layers and a potted housing for the memory device. The CSMM is shown in Figure 17.

Intumescent Shell

The intumescent shell is bonded to the armored housing and forms the exterior of the CSMM. Figure 18 shows the design configuration which was evaluated and subjected to survivability testing. The shell is made up of three layers of vulcanized synthetic rubber containing an intumescent ceramic material and includes a wire mesh reinforcement between the outermost and middle layer of rubber. The shell consists of two pieces, a flat cover and a rectangular box. The overall thickness on any side is 0.25 inch. In the assembled state, the wire mesh in the cover and in the rectangular box are bonded together to provide continuous reinforcement around the CSMM periphery.

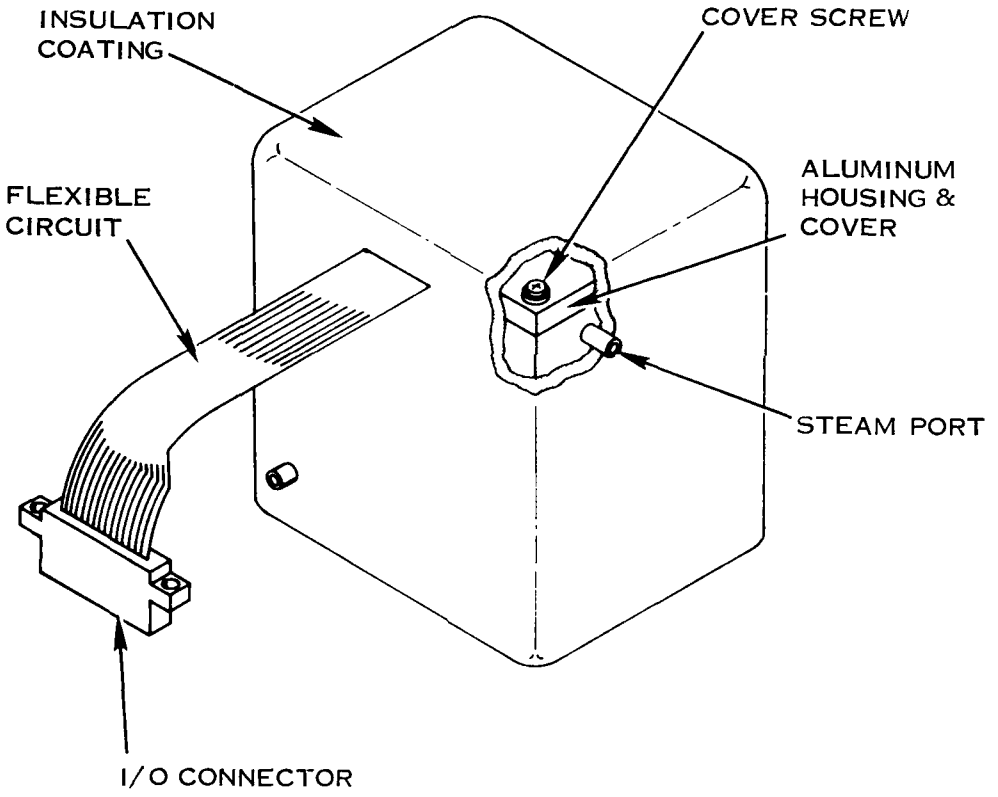


FIGURE 17. AIRS CSMM

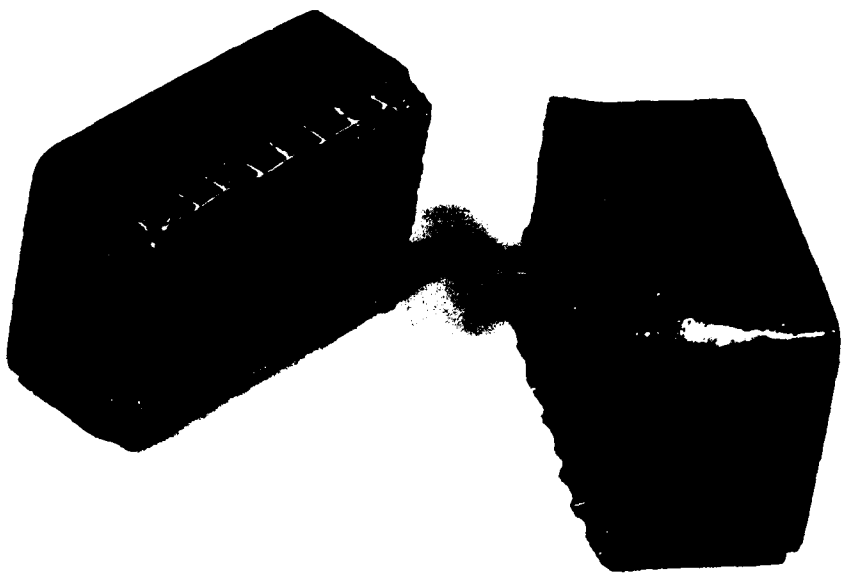


FIGURE 18. AIRS INSULATING SHELL - CENTER SEAM

The intumescent shell provides the initial thermal barrier to 1100°C flame resulting from an aircraft aviation fuel fire. The insulating shell begins to intumesce at approximately 500°C. As the flame temperature increases to 1100°C, the material forms a tough insulating char which provides a high thermal resistance to protect the memory module from the high external ambient temperature via the process of high surface radiation, absorption of energy through the chemical process of decomposition, and removal of energy through the process of transpiration.

Armored Housing

The armored housing consists of two pieces, a flat cover and a rectangular box. The cover is bolted to the housing with twelve #6-32 socket head cap screws. Both pieces are made from 7075-T6 aluminum alloy and are 0.312 inch thick on all sides. This material and material thickness were selected on the basis of their resistance to penetrating loads and low weight considerations.

Water-Filled Layers

Internal to the armored housing are four separate layers of ceramic fiber insulation. The layers are separated by stainless steel boxes and separator plates. The separator plates are perforated and dimpled. Each layer of ceramic fiber insulation is filled with water during assembly.

The perforations in the separator plates allow water to migrate from one layer to the next during water boil-off and the dimples allow layer expansion to offset effects of water expansion in freezing conditions.

The layers provide thermal protection in a fire in two ways. First, when the module is exposed to fire, the water in the outermost layer will boil and absorb its latent heat of vaporization. As the water boils, steam is vented through two small stainless steel tubes pressed into the housing. After the water in the first layer is completely boiled away, the next layer will begin to boil and the steam generated will migrate through the outer layer and exhaust through the vent tubes. This process occurs sequentially from the outermost to the innermost layer. Secondly, the layers function as insulation once their water is boiled away. In this manner, the thermal resistance from the fire to the boiling water increases as the layers are sequentially boiled away. The inner module temperature never exceeds 100°C (212°F) provided some water remains in the assembly.

The vent tubes are sealed with a fusible metal alloy which melts at 203°F. The vents thus will allow venting of steam when the water internal to the CSMM boils, but will prevent loss of water in normal service. Figure 19 shows the CSMM in its disassembled state showing the four separate water boiler layers.

Potted Memory Module

The potted memory module (see Figure 20) is composed of a silicone closed-cell foam surrounding the memory device and an outside layer of silicone rubber. The memory device is soldered and bonded directly to a flexible circuit and

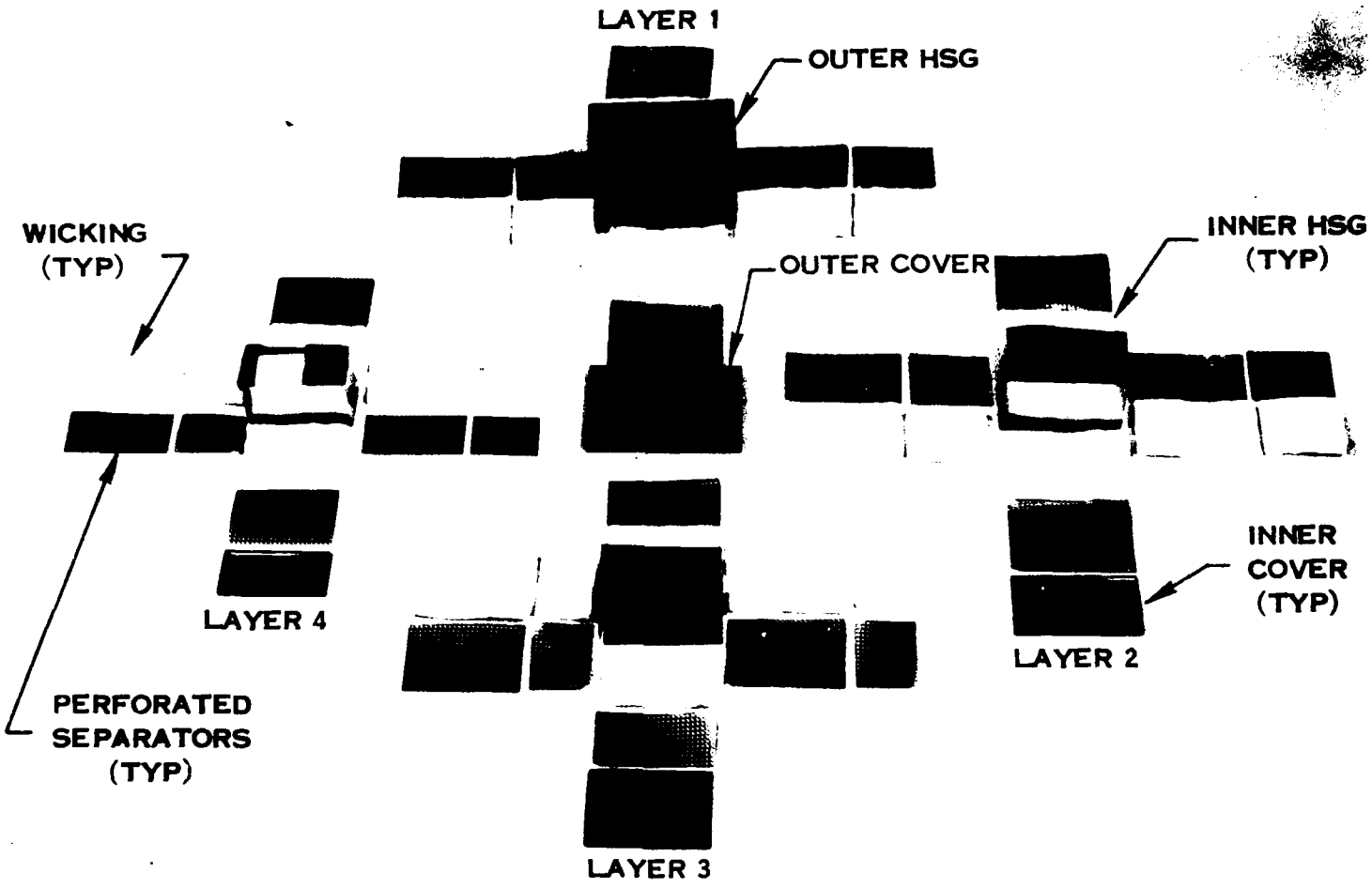


FIGURE 20. POTTED MEMORY MODULE

then is encapsulated in the silicone foam and rubber. The flexible circuit is routed out of the CSMM through the water-filled layers, taking an indirect course to prevent short-circuiting of the thermal protection.

The potted module protects the memory device by isolating it from the water filled environment and by giving it freeze-crush protection. The freeze-crush environment is created when the water in the module goes through the freezing point and its volume increases. This expansion is absorbed partially by the compressible silicone foam in the potted module.

AIRCRAFT INSTALLATION DESIGN DETAILS

The UH-60A BLACK HAWK location recommended for the AIRS unit and the impact accelerometers is on the cabin floor adjacent to the battery (see Figure 21) and enclosed in an enlarged battery box. This location was chosen for the following reasons:

* Survivability: This area has a high structural integrity because it supports the landing gear. Also, it is protected from frontal crash impact damage, tail cone separation, and is not in close proximity to the engines, auxiliary power unit (APU), and fuel tanks.

* Operational: The rigid floor structure and high integrity of this area, coupled with close proximity of the AIRS, the power source, and the accelerometers, allow maximum functional survivability through a crash impact. The close proximity of the accelerometers to the landing gear allows analysis of landing gear shock absorption and severity of fuselage impact. Their close proximity to the crew seat mountings allows effective analysis of impact loads on the crew and evaluation of the effectiveness of the energy absorbing seats.

* Cost and Weight: Installing the AIRS unit and the accelerometers close together and adjacent to the power source minimizes the runs on the strengthened cables required for integrity during impact recording. Also, the chosen location is easily accessible for installation and maintenance.

The UH-60A AIRS installation would include the following items:

* AIRS electronics unit

* Accelerometer assembly (3 axis impact, 1 axis flight)

* Rudder pedal position sensor assembly

* Lateral cyclic position sensor assembly

* Airframe wiring, clamps, conduits, connectors and circuit breaker

All other aircraft parameters are available as electrical signals and do not require special sensors.

Figure 21 shows the location in the airframe of the electronics unit and accelerometers. A more detailed layout of these units is shown in Figure 22 relative to the battery. Close proximity to the battery and the short wire run to the accelerometer assembly will maximize functional survivability during impact. For other aircraft, a similar arrangement is recommended.

The control position sensor assemblies would be similar to assemblies currently used to measure control positions as a part of other aircraft systems such as the flight control system. A typical rotary motion sensor installation is shown for both the pedal position and lateral cyclic position sensors (see Figure 23).

The potentiometers and the sheet metal assembly for potentiometer mounting and motion input are the only nonstock parts for these assemblies.

The weight of the installation over and above the AIRS unit and sensors was estimated for the UH-60A aircraft for the chosen location of the AIRS unit and an estimate of the length of wire running to the accessible signal pick-off points. Table 15 summarizes the installation weight data.

As a typical example of the effort required to install AIRS, the installation guidelines were given to the participating airframe manufacturer and a preliminary estimate was prepared. The estimate considered installation both as a retrofit kit and as part of the aircraft during original manufacture.

The recurring man-hour estimate to install the AIRS considered wire runs, numbers of wires, clamping, armoring, unit and sensor installations, bracketry, threaded floor receivers, connectors, etc.

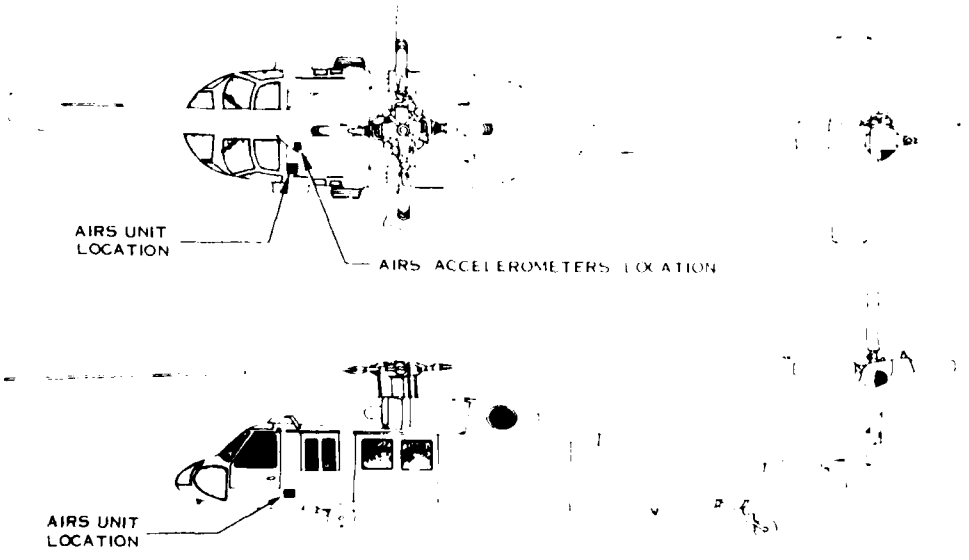


FIGURE 21. TYPICAL AIRS COMPONENTS LOCATION

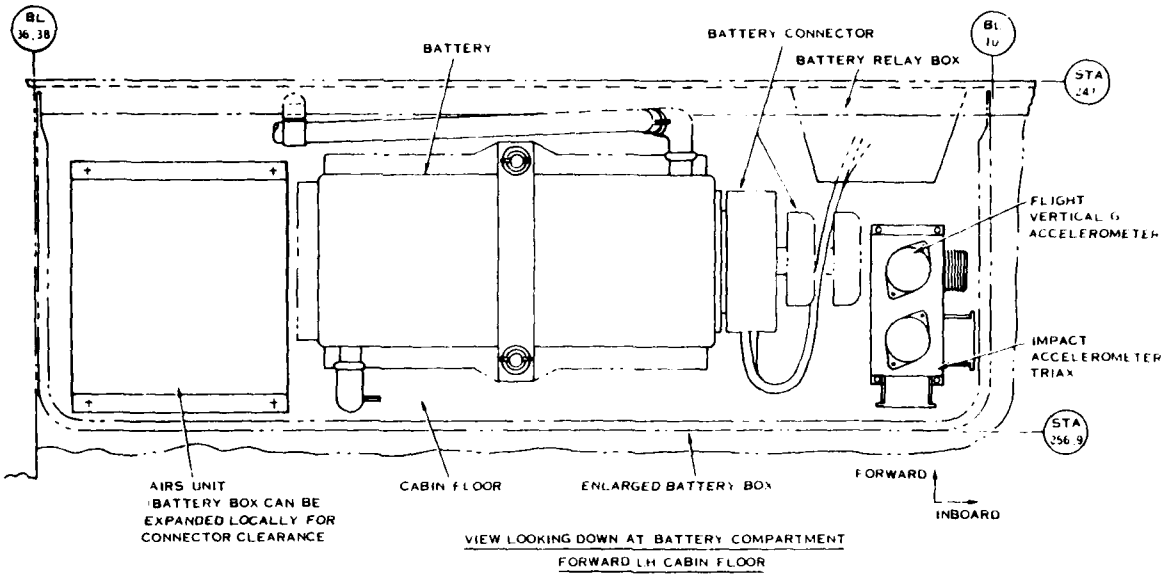


FIGURE 22. TYPICAL AIRS UNIT INSTALLATION

6
B

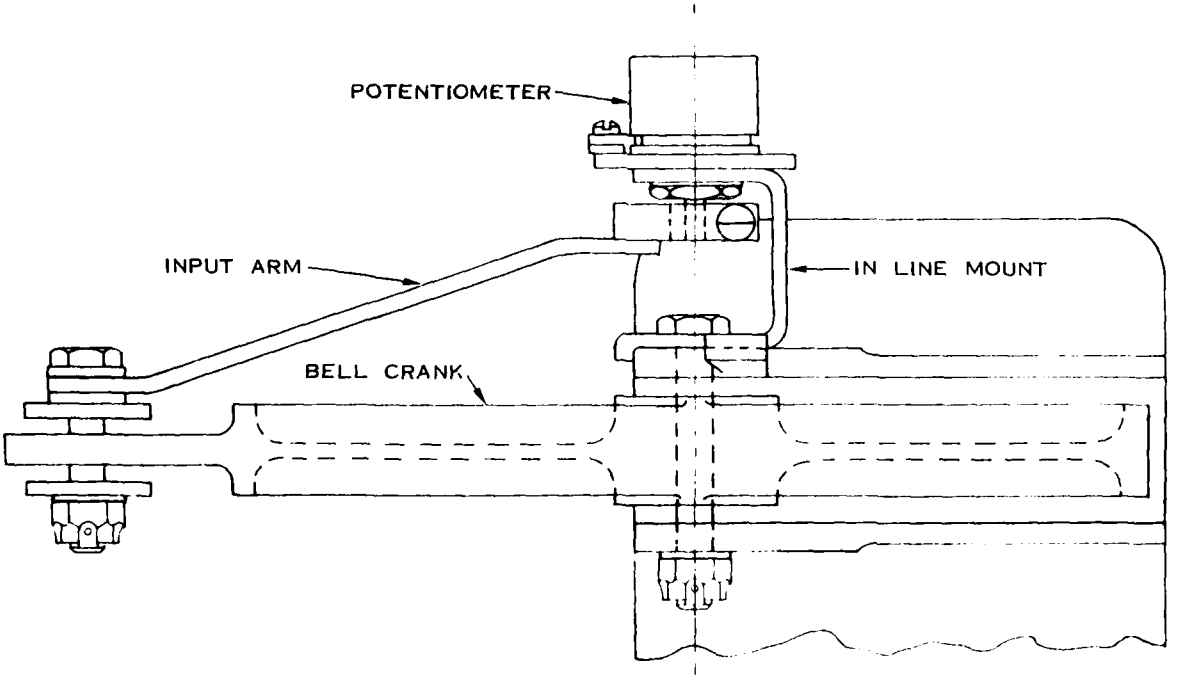


FIGURE 23. ADDED CONTROL POSITION SENSORS

TABLE 15. ESTIMATE FOR UH-60A APPLICATION INSTALLATION WEIGHT

(Not including AIRS unit and sensors)

ITEM	WEIGHT (POUNDS)
Threaded floor receivers (AIRS unit and accelerometer unit)	0.8
Extended battery cover door AIRS units	0.3
Armored cable and brackets (Power line and accelerometer lines)	0.42
Local circuit breaker	0.06
Wiring harness and brackets (All number 24 gauge-shielded except discrete signal leads)	3.0
Lateral cyclic and pedal position sensors link and mounting bracket	0.8
TOTAL	5.38

The estimate also considered standard learning curve factors for typical lot buys of systems and installation. Figure 24 summarizes the estimate findings.

It should be noted that proper provisioning of the aircraft in terms of pre-wiring, space, and mounting bolt threaded receivers in place in the floor will reduce the after-aircraft manufacture AIRS installation effort down to a value approximately that of the lower curve shown.

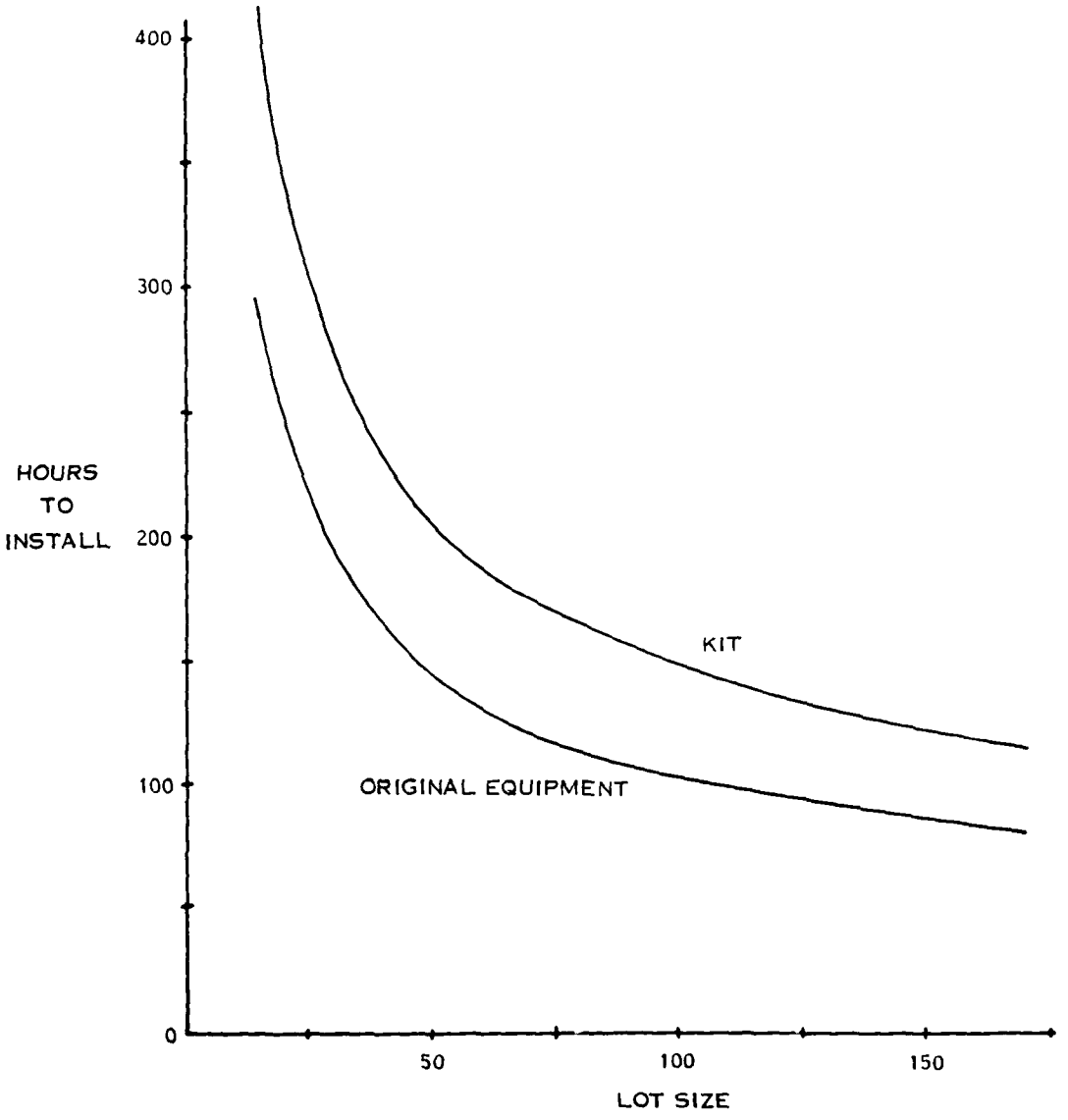


FIGURE 24. TYPICAL AIRS RECURRING EFFORT FOR INSTALLATION

RELIABILITY

The AIRS design will meet or exceed the requirements set forth in the Reference 1 study report thus providing an enhanced logistical system. The prime reliability factors and design features which will optimize the AIRS are:

* Design service life equal to or greater than 8,400 hours.

* Minimization of custom hybrids.

* Maximum use of proven circuitry.

* Maximum use of monolithic integrated circuits.

* Component derating guidelines which meet or exceed military requirements

* Priority selection of high reliability parts.

The reliability estimates calculated used the following factors and assumptions:

1.	Ambient temperature	100°C
2.	Voltage Stress	30%
3.	Power Stress	30%
4.	Duty Cycle	100%
5.	Failure Rate Source	MIL-HDBK-217C
6.	Part Levels	
	Semiconductors	JTX, JN
	Integrated Circuits	883B
	Hybrid Memory	Per MIL-HDBK-217C
	Resistors	ER
	Capacitors	ER
7.	Reliability Equation	$T = \lambda 1 + \lambda 2 + \ldots + \lambda n$

Results of the reliability calculations were as follows:

AIRS Unit	$\lambda(10^6$ hr)	MTBF (hr)
Analog Conditioner	14.53	
Frequency I/O & Processor	20.74	
Power Supply	14.32	
Hybrid Memory Interface	5.36	
Hybrid Memory	27.01	
Interconnections (misc)	15.00	
Subtotal	96.96	10,300

SENSOR ADDITIONS TO BLACK HAWK

Accelerometers (4)	12	
Potentiometers (2)	10	
Subtotal	22	45,450
TOTAL	118.96	8,400

DEVELOPMENT HARDWARE, DESIGN, FABRICATION, AND TEST

AIRS BRASSBOARD UNIT DESIGN

For the purpose of developmental testing, brassboard AIRS hardware was designed. The brassboard AIRS was designed to be functionally equivalent to the production configuration with the following added capabilities.

* The AIRS brassboard allows interfacing with the Westinghouse BORAM system in addition to the Hamilton Standard developed hybrid memory.

* Added program and scratch-pad memory was added to allow greater software capability for development testing and software debugging.

* The CSMM was not part of the brassboard; instead, the memory device was mounted directly on the Memory Control card.

* A digital flight data Quick Access Recorder (QAR) interface was provided for recording the continuously sampled AIRS data to provide a baseline against which to compare the reconstructed memory device compressed data.

Two AIRS brassboard units were fabricated and underwent functional and environmental tests to verify their operation and flightworthiness in the expected helicopter environment.

A test rig simulating aircraft signals that would be applied to the AIRS unit during flight was fabricated and used for the testing and verification of the AIRS unit in laboratory testing and to support flight test activities at Sikorsky's experimental flight test center in West Palm Beach, Florida.

The brassboard AIRS unit is shown in Figure 25. The unit measures 8 inches wide X 10 inches high X 10-1/4 inches deep and weighs approximately 15 pounds. The AIRS brassboard contains six wire-wrapped circuit boards and one four layer printed circuit board. The partitioning of the brassboard is as follows:

* Power Supply (WW)

* DC Analog Conditioner (WW)

* Synchro and Discrete (WW)

* I/O and Frequency Board-A (WW)

* I/O and Frequency Board-B (WW)

* Memory Control (WW)

* Processor (PC)

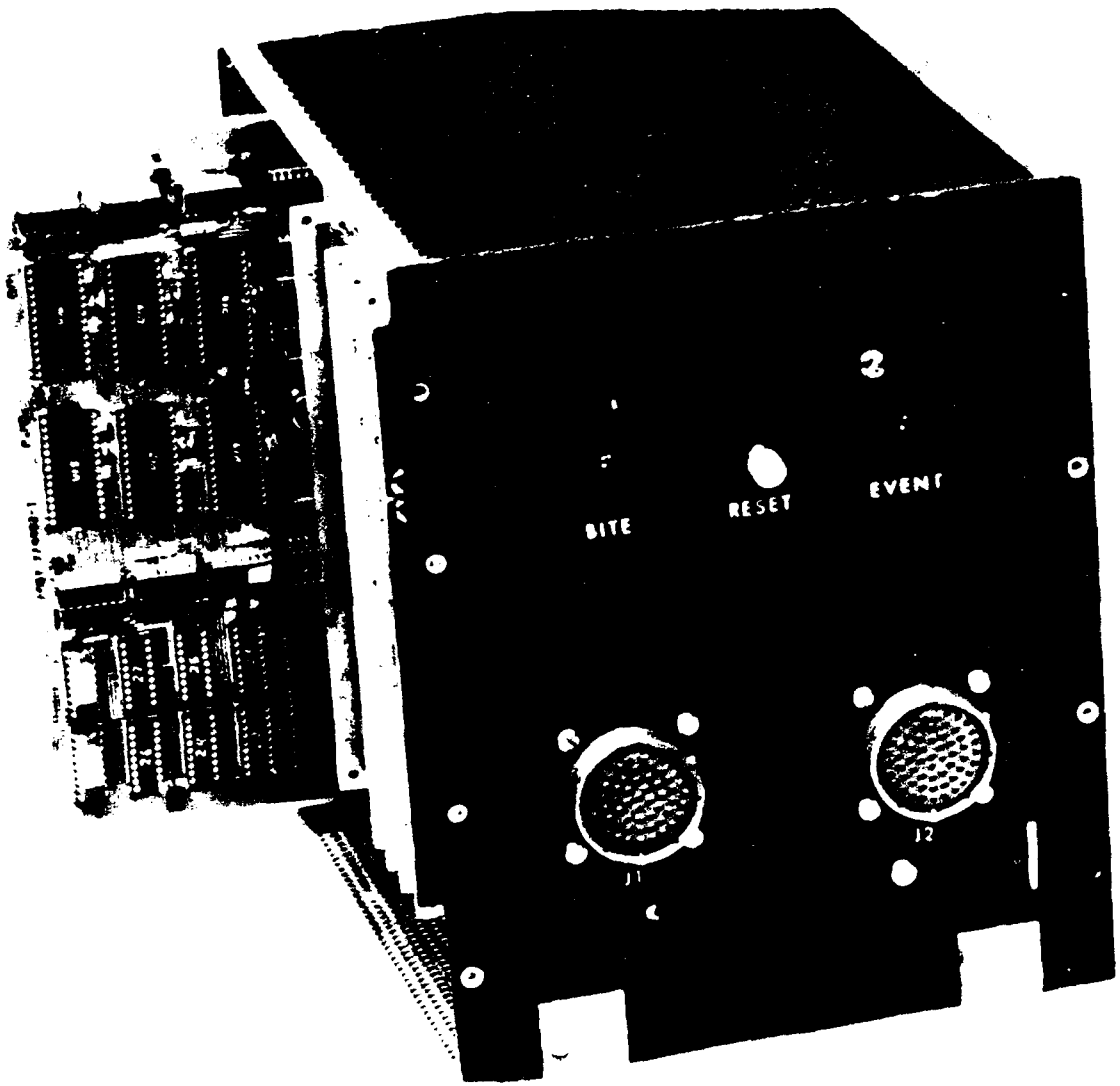


FIGURE 6. [illegible] BRASSBOARD [illegible]

The brassboard unit was shock mounted for flight tests and the chassis ventilation openings allowed convection cooling of the AIRS electronics.

AIRS TEST RIG

General Description

An AIRS test rig was designed and fabricated to provide the means to functionally test the AIRS under simulated operational conditions in the laboratory environment and to support development testing including hardware and software development, flightworthiness assurance tests, and field preflight and postflight test activities.

The AIRS test rig simulated the aircraft signals that would be applied to the AIRS unit during flight. The test rig is comprised of the following component sections (see Figure 26):

1) Power supplies

2) Standardized processor board

3) Analog data board

4) Scaling card

5) Front and rear panel controls

The test rig contains +5 volt and ±15 volt power supplies with jacks for external -20 volt and +28 volt supplies located on the rear panel. The +28 volt supply, controlled via the front panel, is the main source of power for the AIRS unit. The -20 volt supply is used by the test rig to generate ±15 volt DC signals.

Software control of the test rig is provided by an Intel 8085 microprocessor located on the standardized processor board. There are 4K bytes of on-board RAM, 6K bytes of on-board PROM, and sockets for an additional 6K of PROM. The resident monitor is contained in the first 2K bytes while the test software resides in the remaining 4K bytes of installed PROM.

The analog data card contains two digital-to-analog converters that allow software to control time-varying DC signals. This card also contains an analog-to-digital converter with 16 input channels to monitor the final DC output signals. This would allow for a self-test program to check the test rig.

The scaling card takes the output of the D/A converter and scales it into the proper range for each DC signal. It also allows a common mode voltage to be applied to the high and low sides of an output signal.

All operator control is implemented through the use of switches located on both the front and rear panels or by entering software commands via a CRT. The AIRS test rig is depicted in Figure 27.

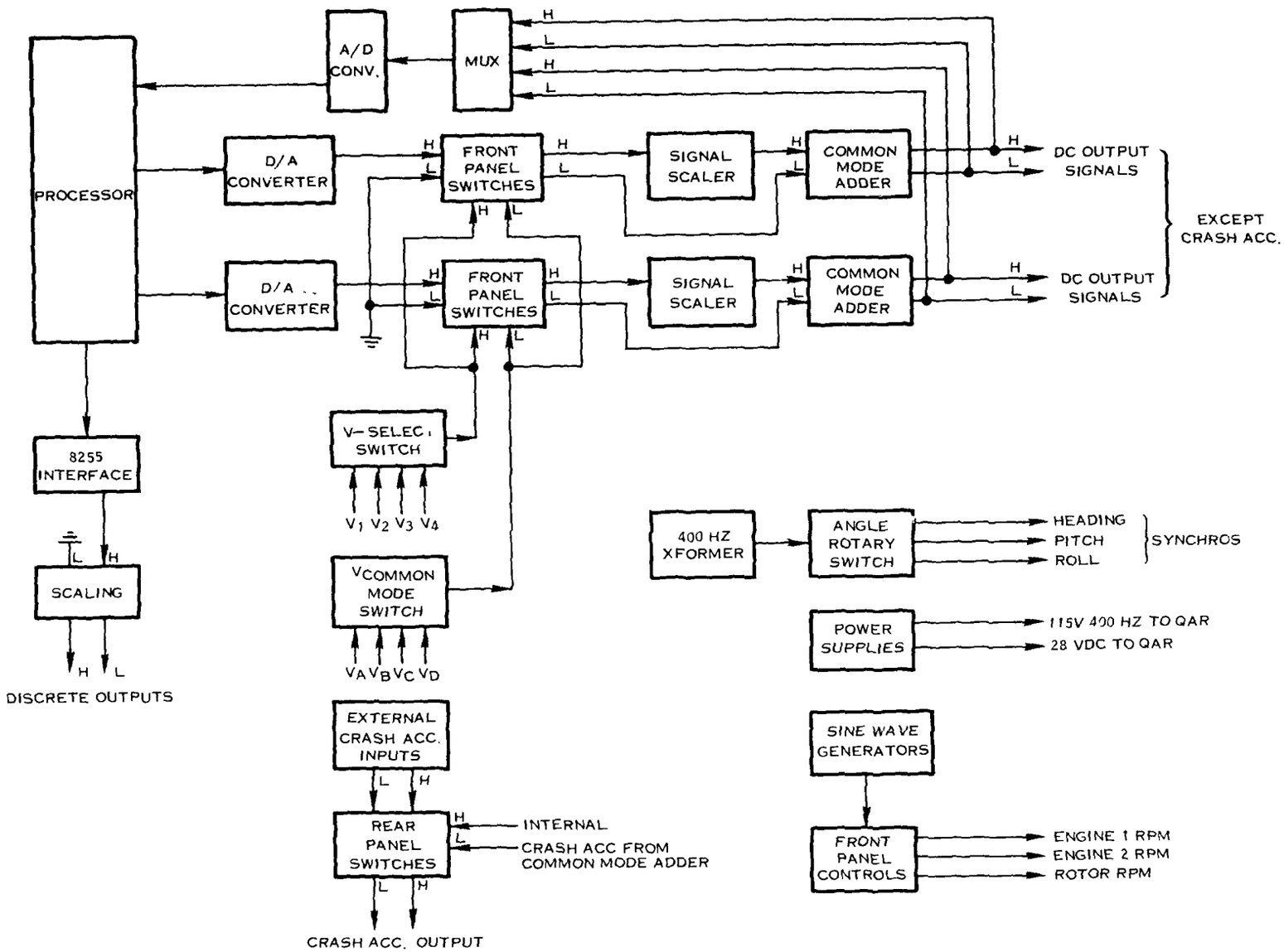


FIGURE 26. AIRS TEST RIG BLOCK DIAGRAM

FIGURE 27. ATRS TEST EQUIPMENT

DC Signals

A list of available DC signals and their respective output ranges is presented in Table 16. Two methods exist in the test rig to vary any or all of these signals. The first (D/A mode) method employs two twelve bit digital-to-analog converters located on the analog data board. These D/A's can be accessed statically using the resident monitor or the test software. The test software can also vary the D/A output dynamically, depending on the command issued. The second method (select mode) uses a four-position rotary switch to select a predetermined output voltage. This allows an easy static check of each DC signal channel. There are also four common mode voltages which can be scaled to any signal in this mode of operation.

The unscaled voltage for each DC signal, produced by either method, is fed into a two-stage operational amplifier network located on the scaling card. The first stage scales the voltage so that +10 volts (D/A full scale output) creates a maximum final output voltage. The second stage allows a common mode voltage, selected via the "V-common mode" rotary switch, to be added to any signal operating in the select mode. The common mode voltages available are +5 VDC, $\pm$5 VAC, 400 Hz, and ground. Any signal in the D/A mode will always have a common mode voltage of 0. The final scaled and summed signal is delivered to the AIRS box through the J2 cable.

The three crash accelerometers differ from the other DC signals only in the select mode. Each has its own 10 turn pot to vary the output over its entire range rather than operate from the four-position rotary switch.

Three switches and associated jacks located on the rear panel allow the internal impact accelerometers to be disabled and external accelerometers to be used for testing.

Discrete Signals

The discrete signals available on the test rig are listed in Table 17 along with their respective set/reset voltages. The discretes are operated by software communication with an Intel 8255 - a programmable peripheral interface located on the scaling board. The output of each 8255 bit is scaled to the correct set/reset voltages by an operational amplifier and channeled to the AIRS unit through the J1 cable.

The level of each discrete can be programmed by the resident monitor, by a user entered program or by running the test software using the proper commands.

Synchro Simulators

There are two modes of synchro simulation available to the operator. The first method employs circuitry internal to the test rig and allows a selection between 1 of 4 angles to be output to the AIRS unit. The other method is to use an external synchro simulator in conjunction with the test rig to allow angle selection from 0 to 360^{o}.

TABLE 16. AIRS TEST RIG DC SIGNALS

SIGNAL	VOLTAGE RANGE
Airspeed	±10
Longitudinal Stick Position	±1.2
Vertical Flight Accelerometer	±2.5
Collective Stick Position	±5
Lateral Stick Position	±5
Pedal Position	±5
Stabilator Actuator 1	±5
Stabilator Actuator 2	±15
Engine Torque 1	±5.277
Engine Torque 2	±5.277
Ice Rate	±5
Altitude Rate	±5
Vertical Impact Accelerometer	±10
Lateral Impact Accelerometer	±10
Longitudinal Impact Accelerometer	±10

TABLE 17. AIRS TEST RIG DISCRETES

SIGNAL	VOLTAGE LEVELS
Chip Detect 1	0/28
Chip Detect 2	0/28
Hydraulic Pressure Engine 1	0/28
Hydraulic Pressure Engine 2	0/28
APU Pressure	0/28
Spare #1	0/28
Spare #2	Gnd/OC
Event	Gnd/OC
Maintenance Readout Unit	Gnd/OC
Portable Ground Test Unit	Gnd/OC
Spare #3	Gnd/10
Spare #4	Gnd/10
Encoded Altitude (9 Bits)	0/15
SAS Fault	0/28
SAS/FPS Fault	0/10 (20 Msec)
Fire Detect	0/28

To use the internal synchro simulators, the INTERNAL/EXTERNAL switches, located on the front panel, must be placed in the INTERNAL position. The angle signal sent to the AIRS unit is now determined by the position of the "Angle" rotary switch. A 115V, 400 Hz to ±5.1V and 26V, 400 Hz synchro transformer inside the test rig provides the three voltages necessary to simulate synchro signals. The ±5.1 voltages and ground are wired to the angle select switch that creates different combinations of XY, XZ and YZ signals that determine the synchro angle.

An external synchro simulator can be used by placing the internal/external switches in the external position. The output of the simulator is connected to the input test jacks, located under each internal/external switch, and the reference input of the simulator is connected to the 26V reference output of the test rig. The attitude angle is now determined by the external synchro settings.

Engine Speed Simulator

The AIRS test rig contains three sine wave generators which are used to provide the Engine 1, Engine 2, and Rotor speed signals. Each generator contains a comparator/operational amplifier circuit whose output is a constant amplitude triangular wave. This triangular wave is passed through a diode network which rounds off the peaks and causes the waveform to approximate a sine wave through a variable gain operational amplifier. The sine wave has a frequency range of 150 Hz to 23 KHz with an amplitude range from 2 VPP to 20 VPP. The coarse frequency, fine frequency, and amplitude controls are located on the front panel.

Software Description

In the test rig, there are two programs burned on PROM. The first 2K bytes of memory contain the resident monitor which is used to start the test software. The monitor also allows the user to enter his own mini-test routines as necessary. There are seven commands of interest in this application.

Display: D START ADDRESS , END ADDRESS

This command displays the contents of the requested memory locations on the CRT.

Substitute: S ADDRESS

Changes contents of specified memory address.

Fill: F START ADDRESS , END ADDRESS , DATA BYTE

Fills a block of memory whose boundaries are given by START ADDRESS and END ADDRESS with the specified data byte.

Go: G ADDRESS

Transfers program control to the specified address.

Go - Break: G ADDRESS SPACE- BREAKPOINT SPACE- BREAKPOINT

Similar to the Go command except that the monitor will resume control when a breakpoint is reached. The instruction is not executed and the break does not affect current 8085 registers.

Register Display: X

Displays current 8085 register contents.

The next 4K of memory contain the AIRS test software starting at location 800H. To get into the test software from the monitor, G800 must be entered. The valid commands available to the user are listed below along with their associated syntax.

Help Help

Displays all of the valid commands on the CRT.

Mon Mon

Transfers program control back to the resident monitor.

Summation Sum

Displays current logic levels of all discretes except the 50ms SAS. This signal is normally logic 0.

D/A Calibration D/A Cal.

Subroutine for calibrating the D/A converter.

Abort ABO

Aborts current task. Test software retains program control.

Limit Exceedance LESSSCCC

Causes the selected DC signal output to ramp upward over 1.5 minutes. The last step forces the output to be greater than the signal's limit exceedance value.

SSS = Any number of spaces

CCC = Signal name. (Table 18)

Encoded Altitude EA876543210

TABLE 18. AIRS TEST RIG LIMIT EXCEEDANCE SYNTAX

SIGNAL	MINIMUM IDENT
Longitudinal Stick Position	LO
Vertical Flight Accelerometer	V
Collective Stick Position	C
Lateral Stick Position	LA
Pedal Position	P
Stabilator Actuator 1	S1
Stabilator Actuator 2	S2
Engine 1 Torque	E1
Engine 2 Torque	E2
Ice Rate	I
Altitude Rate	AL
Encoded Altitude	EA
Airspeed	AI

7
F

Sets the nine encoded altitude bits to the specified value.

Test Conversion TCSSSCC

Performs an analog-to-digital conversion of the output signal specified by CC (Table 19).

Discrete Set/Reset

Programs the desired discrete logic level. Table 20 contains syntax for each discrete.

Peak High PH

Causes D/A #1 to generate a one-cycle square wave output whose maximum count is 3FFH and whose minimum count is 00FFH. Maximum absolute transition is positive and its period is approximately 0.22 sec.

Peak High Continues PHC

Same as peak high except that the D/A output is a repetitive square wave.

Peak Low PL

Same as peak low except that the D/A output is a repetitive square wave.

D/A Set SD/ANSSXXXX

Sets the value of the selected digital-to-analog converter. 7 B

N = D/A Number (1 or 2)

SS = Spaces

XXXX = Four-digit hex value

Identify D/A ID/A

Shows which D/A controls each signal in the D/A mode. Table is displayed on the CRT.

BRASSBOARD FUNCTIONAL TESTS

Prior to the start of flight testing, the AIRS brassboard electronics unit was subjected to operational development tests to verify functional operation of the electronics.

The development tests performed are summarized as follows:

* Power Supply Tests
  - Power Dissipation
  - Internal Voltages

TABLE 19. AIRS TEST RIG TEST CONVERSION CHANNELS

SIGNAL	CHANNEL
Lateral Stick Position	00
Ice Rate	01
Engine 2 Torque	02
Engine 1 Torque	03
Longitudinal Stick Position	04
Collective Stick Position	05
Pedal Position	06
Altitude Rate	07
Vertical Impact Accelerometer	08
Lateral Impact Accelerometer	09
Longitudinal Impact Accelerometer	0A
Airspeed	0B
Stabilator 1	0C
Stabilator 2	0D
Vertical Flight Accelerometer	0E

TABLE 20. AIRS TEST RIG DISCRETE SET/RESET

Syntax: Set Discrete High

CCC1

: Set Discrete Low

CCC0

CCC = Discrete Identification

DISCRETE	IDENTIFICATION (CCC)
Fire Detector	FD
Chip Detector 1	CD1
Chip Detector 2	CD2
APU Pressure	APU
Spare #1	SPR1
Spare #2	SPR2
Event	EV
Maintenance Readout Unit	MR
Portable Ground Test Unit	PGU
Spare #3	SPR3
Spare #4	SPR4

* Processor Tests

  - Internal Frequency
  - Power Up/Power Shutdown Sequence
  - Data Sampling and Recorder Storage
  - EAROM Data Storage Protection of Event in EAROM
  - EAROM Dump to Recorder
  - Instruction Set Verification
  - Interrupt Routines
  - EAROM Memory/RAM Verification

* Input Signal Conditioning Tests

  - Analog Signals
  - Input Filtering
  - Impact Signal Monitoring
  - Discrete Signals

* EAROM Instruction Set

  - Read Current Address
  - Increment Address and Read
  - Decrement Address and Read
  - Test Current Address
  - Increment Address and Test
  - Decrement Address and Test
  - Write Current Address and Increment Block
  - Set Protect
  - Reset Protect Flag
  - Clear FIFO

Power Supply Tests

The power supply tests consisted of measuring the input power at various input voltages and measuring internal voltages and characteristics. These were found to be within the limits as specified in Table 21.

Processor Tests

The processor tests consisted of verifying the central processing unit (CPU) clock frequency and all processor operations. These include tests verifying power up, start-up and shutdown routines plus all normal interrupt and test routines. All processor operations were determined to be acceptable.

Input Signal Conditioning Tests

The input signal conditioning tests verified that simulated input signals were conditioned such that the system interpreted them correctly. These tests were accomplished by verifying that the input correlated with the digital output. All signals were determined to be within limit.

TABLE 21. POWER SUPPLY TEST LIMITS

Input Power	Limit	
@ 20 VDC, 24 VDC, 28 VDC	Less than 35 watts	
Internal Voltages (Measured at 20 VDC and 28 VDC input)	**Accuracy**	**Maximum Ripple**
+5 VDC	±5%	50mV
+10 VDC	±5%	10mV
+15 VDC	±5%	50mV
-10 VDC	±5%	10mV
-15 VDC	±5%	50mV
-20 VDC	±5%	10mV

EAROM Instruction Set Test

In this test, eleven EAROM operations were exercised. These included addressing, reading, writing, testing, protecting and reset. These operations were verified to be functioning normally.

BRASSBOARD FLIGHTWORTHINESS TESTS

Flightworthy assurance tests were performed on the AIRS brassboard flight unit. These environmental tests assured that the electronics unit will function as desired while on board the aircraft during flight testing. The tests included:

* Temperature Tests
* Vibration Tests
* Shock Tests
* EMI Tests

Temperature Tests

The test item was subjected to temperature testing which consisted of five cycles through a temperature range of -10°C to +60°C. Test item operation was noncontinuous. At selected points in the temperature cycles, selected functional tests were performed to verify proper operation. The test item was found to function properly throughout the test.

Vibration Tests

The test item was subjected to vibration tests consisting of sinusoidal vibration of 2g at a frequency from 5 to 500 Hz. This vibration was applied separately to each of the three mutually perpendicular axes.

During the initial vibration test on the X (vertical) axis, the test item ceased functioning at about 50 Hz and the test was terminated. Inspection of the test item revealed that the processor board had been vibrated free from its interface connector. The processor board was secured with a bracket bolted to the chassis, the unit reassembled, and the test restarted from the beginning. The test item was operationally checked before and after vibration in each axis and the operation monitored throughout the testing. The testing was completed successfully without further incident.

Shock Tests

The test item was subjected to nonoperating shock testing. The test involved six shocks, one shock in each direction along each of the three mutually perpendicular axes with one exception. The +X axis was not accomplished due to the inability to mount the test item on the shock machine in the required orientation. Following each shock, visual inspection of the test item revealed no damage. After completion of the shock testing, the test item was functionally checked and found to be operating properly.

Electromagnetic Interference Tests

The following MIL-STD-461A, Notice 4 tests were performed on the test item.

CE01 - Conducted Emissions on DC Power Leads, 30 Hz - 50 KHz

CE04 - Conducted Emissions on Power Leads, 50 KHz - 50 MHz

CS01 - Conducted Susceptibility on DC Power Leads, 30 Hz - 50 KHz

CS02 - Conducted Susceptibility on Power Leads, 50 KHz - 50 MHz

The tests were performed in accordance with the procedures defined by MIL-STD-462, Notice 3.

Test Results

The test item performed acceptably throughout the Flightworthiness Tests with two (2) exceptions:

1) During vibration testing, a malfunction occurred as a result of the processor board vibrating free from the chassis mounted interface connector. A modification was incorporated to provide positive pressure for board retention. The test was rerun successfully following this modificaton.

2) Narrow-band conducted emissions exceeded the CE01 and CE04 limits. To achieve CE01 compliance, the power input stage filter must be redesigned to provide additional low frequency attenuation. To achieve CE04 compliance, conductors to the I/O connector must be routed to minimize high frequency cross talk to the filtered power leads. This compliance is not considered significant to the operational capabilities of the AIRS or the instrumentation in the helicopter.

Figures 28 through 33 depict the results of conducted emissions tests. Noncompliant narrow-band conducted emission levels are due to the 40 KHz switching regulator and the 3 MHz digital clock. The test item successfully completed the conducted susceptibility tests.

The sucessful completion of the AIRS brassboard development and flightworthy assurance tests specified, demonstrated that the AIRS functions as required and would perform acceptably in the helicopter flight test envoronment.

CRASH SURVIVABLE MEMORY MODULE (CSMM) SURVIVABILITY TESTS

The criteria governing the CSMM design concept are defined in the FAA requirements for crash recorders contained in Technical Standard Order TSO-C51a. These requirements are tabulated in Table 22.

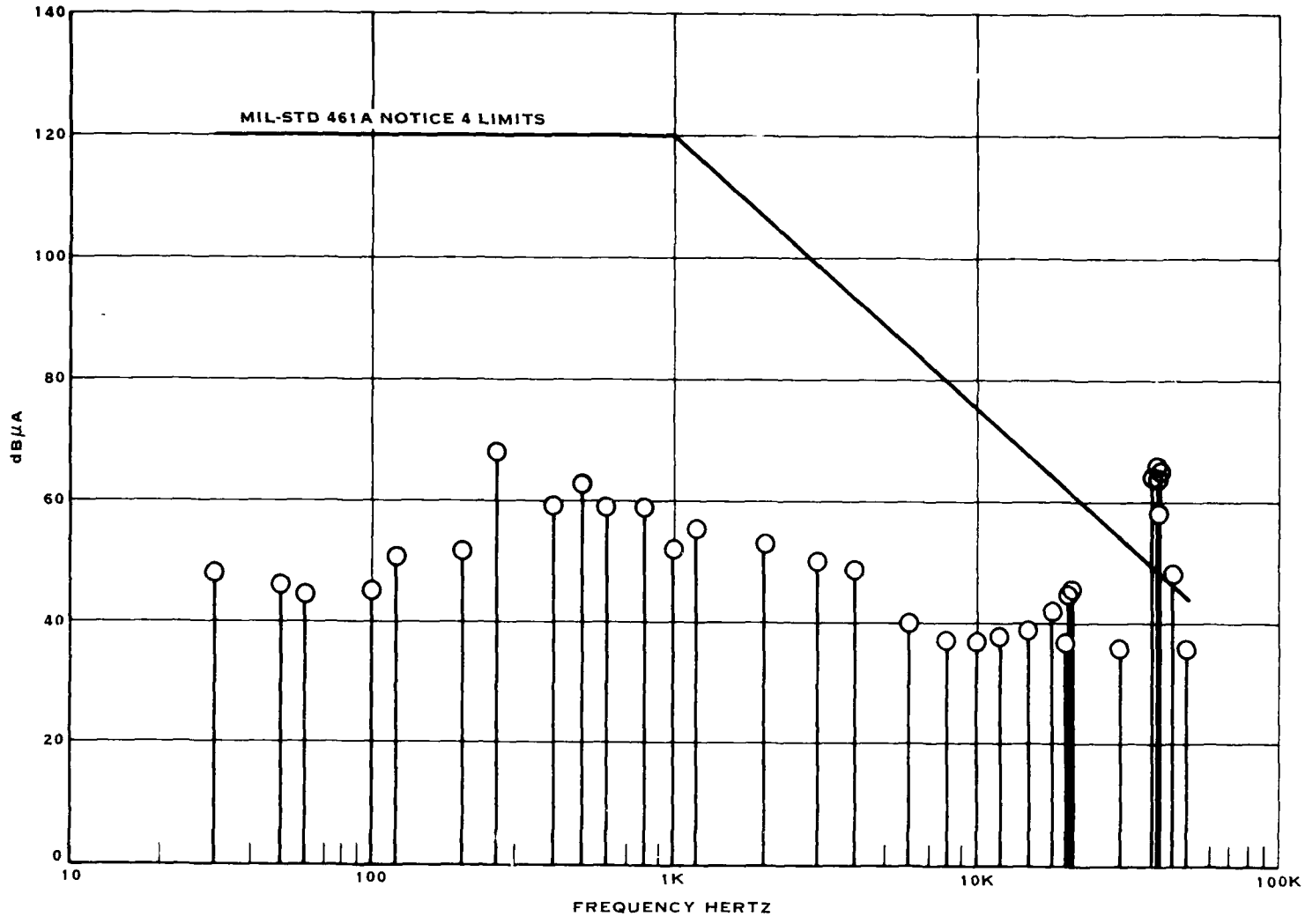


FIGURE 28. NARROW-BAND CONDUCTED EMISSIONS ON THE AIRS 24 VDC POWER INPUT (CEO1 TEST)

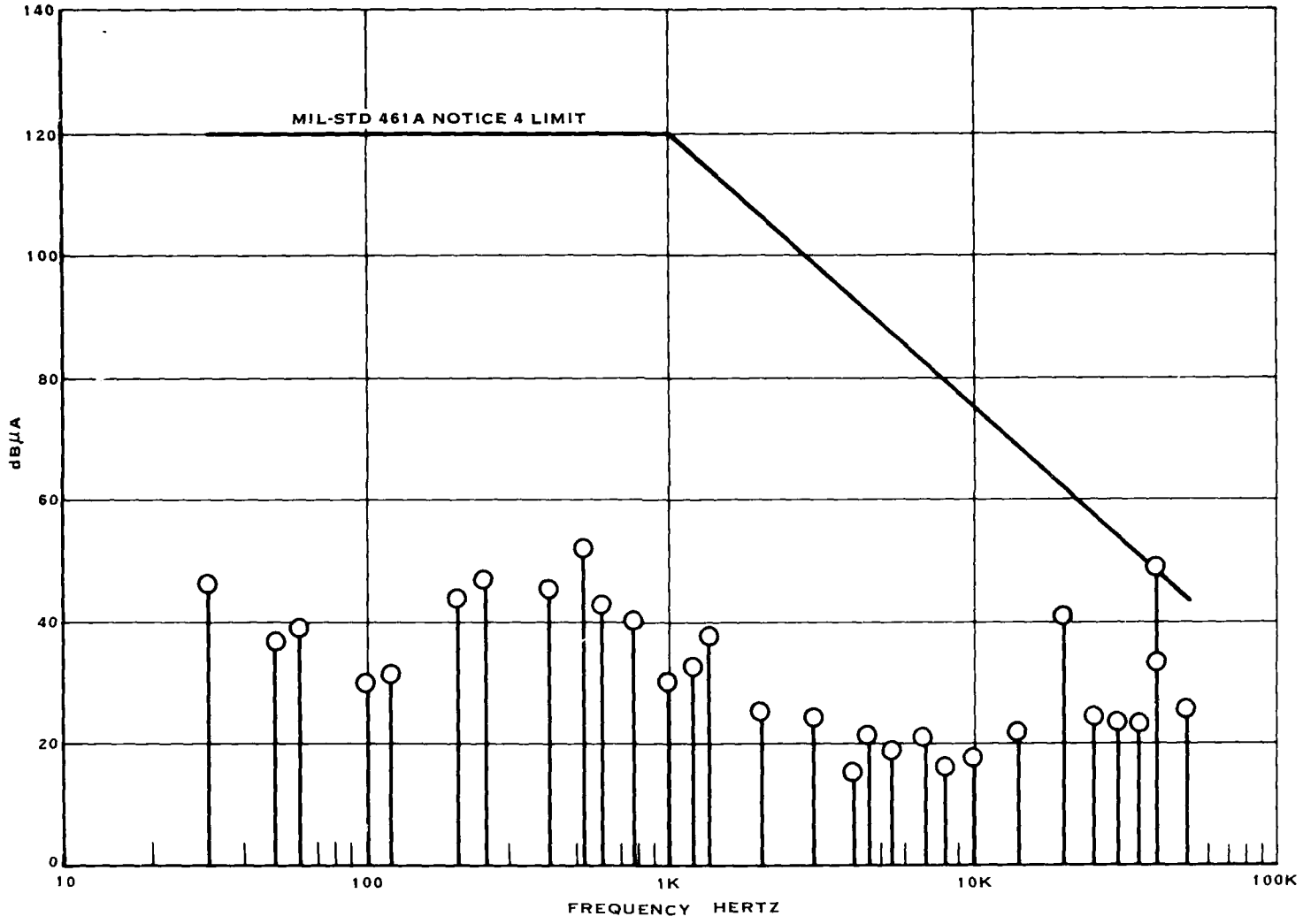


FIGURE 29. NARROW-BAND CONDUCTED EMISSIONS ON THE AIRS 24 VDC POWER RETURN (CE01 TEST)

AD-A105 510 UNITED TECHNOLOGIES CORP WINDSOR LOCKS CT HAMILTON ST--ETC F/G 1/3
ADVANCED CRASH SURVIVABLE FLIGHT DATA RECORDER AND ACCIDENT INF--ETC(U)
AUG 81 H R ASK, D L WHITE, K E BERWICK DAAK51-78-C-0025
UNCLASSIFIED ESP-8109 USAAVRADCOM-TR-81-D-20 NL

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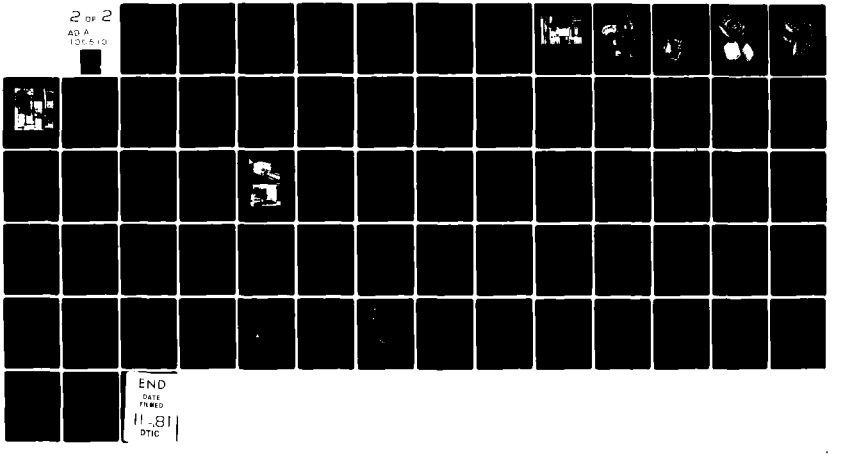
105 510



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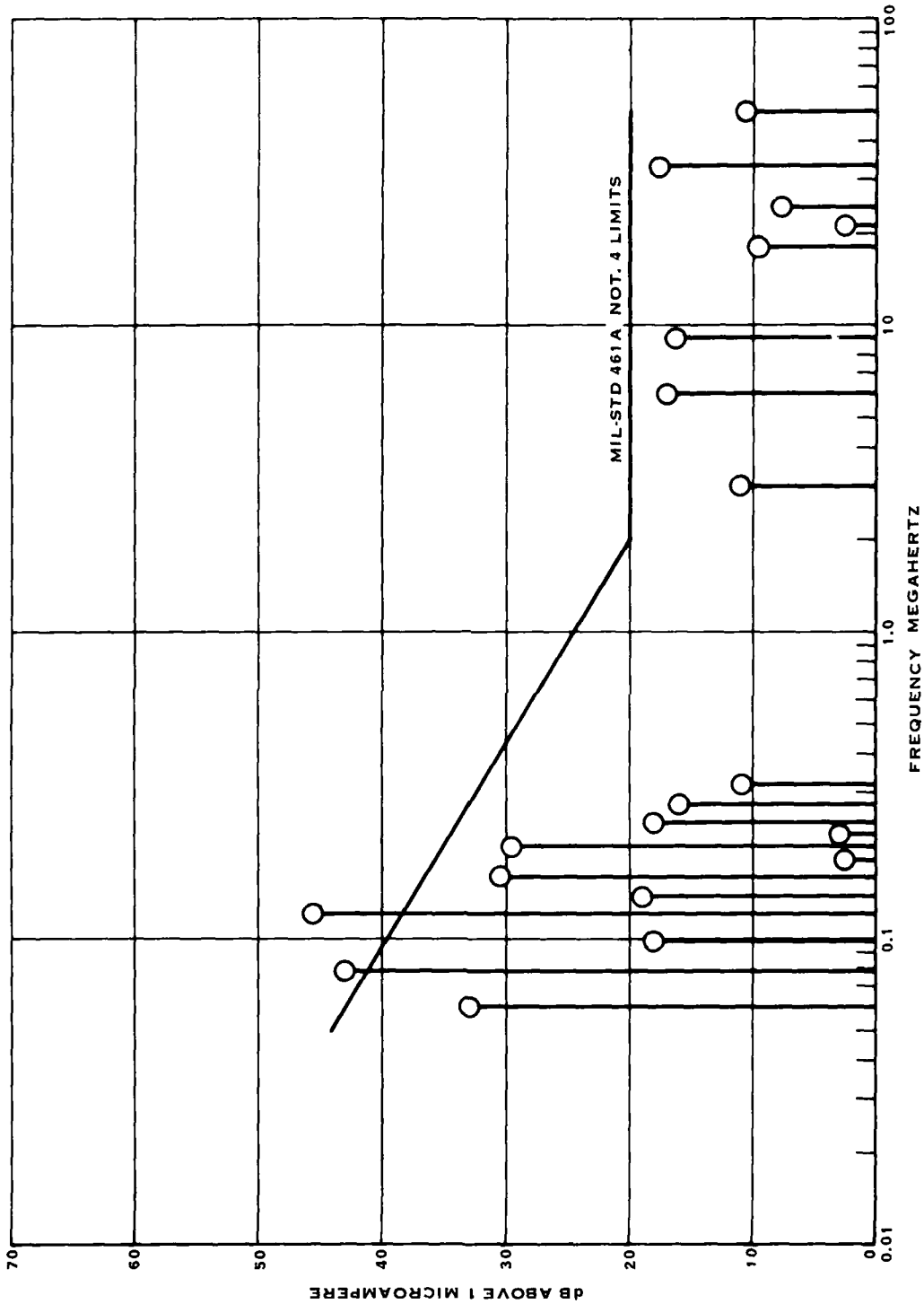


FIGURE 30. NARROW-BAND CONDUCTED EMISSIONS ON THE AIRS 24 VDC POWER INPUT (CE04 TEST)

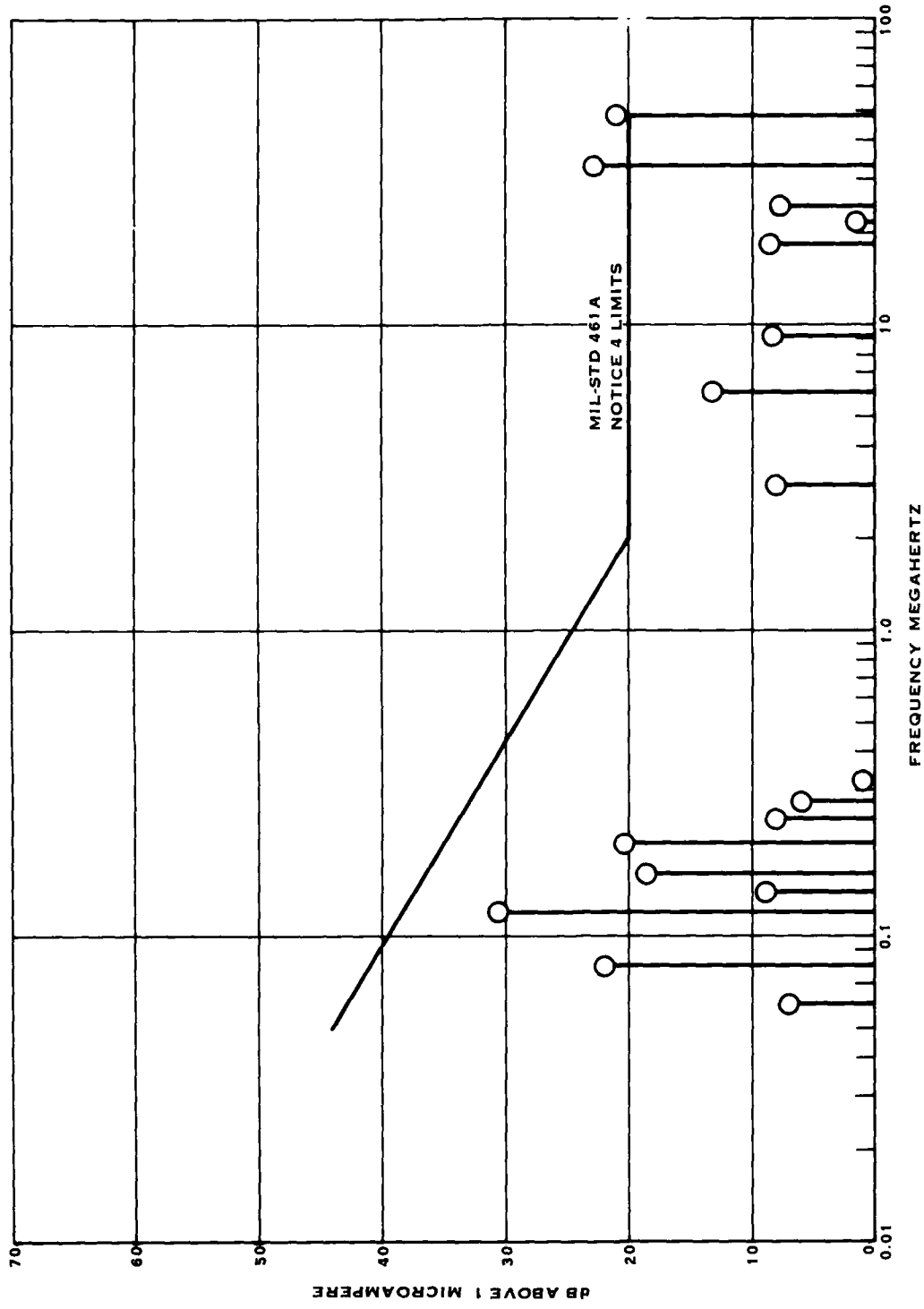


FIGURE 31. NARROW-BAND CONDUCTED EMISSIONS ON THE AIRS 24 VDC POWER RETURN (CE04 TEST)

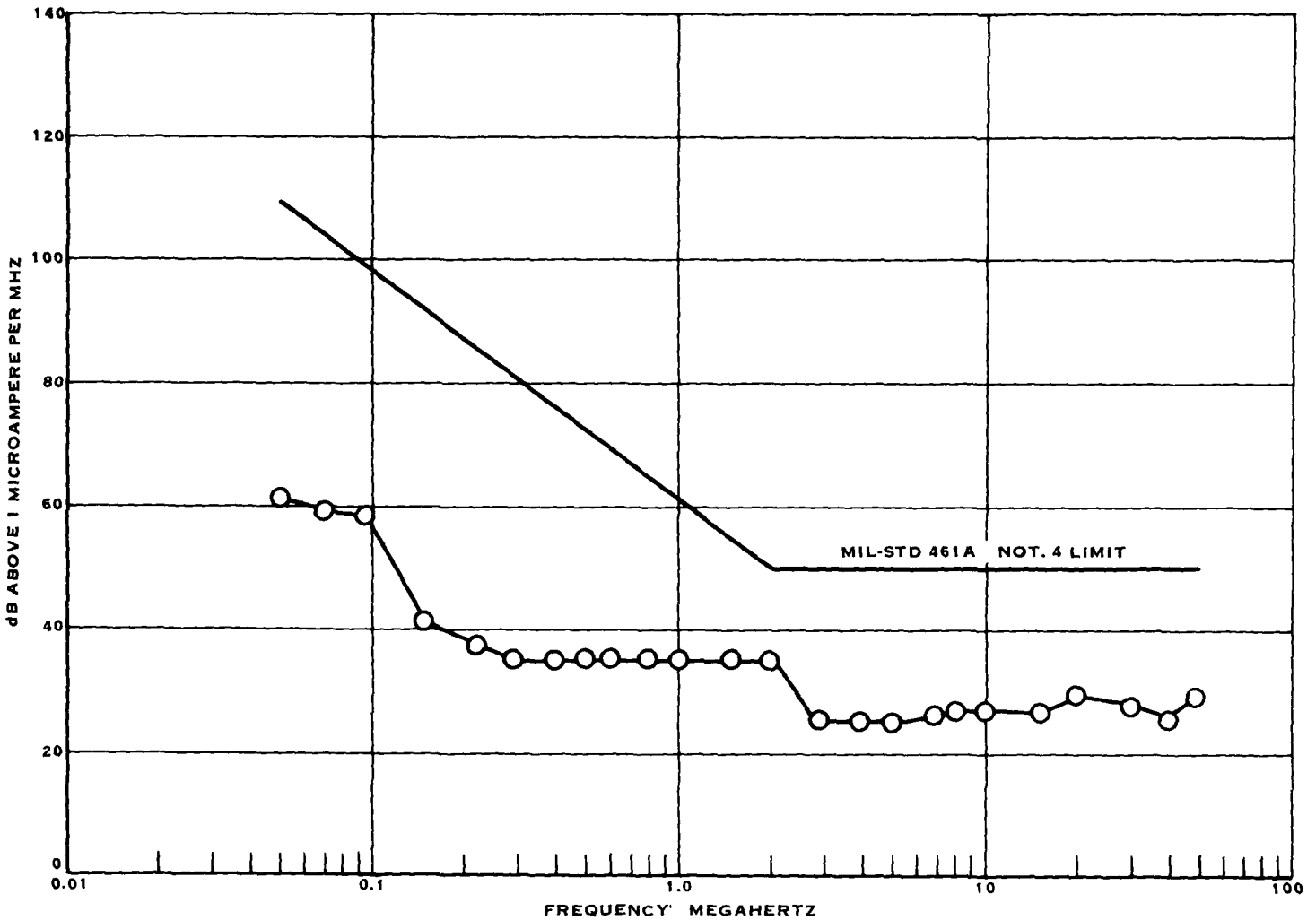


FIGURE 32. BROAD-BAND CONDUCTED EMISSIONS ON THE AIRS 24 VDC POWER INPUT (CE04 TEST)

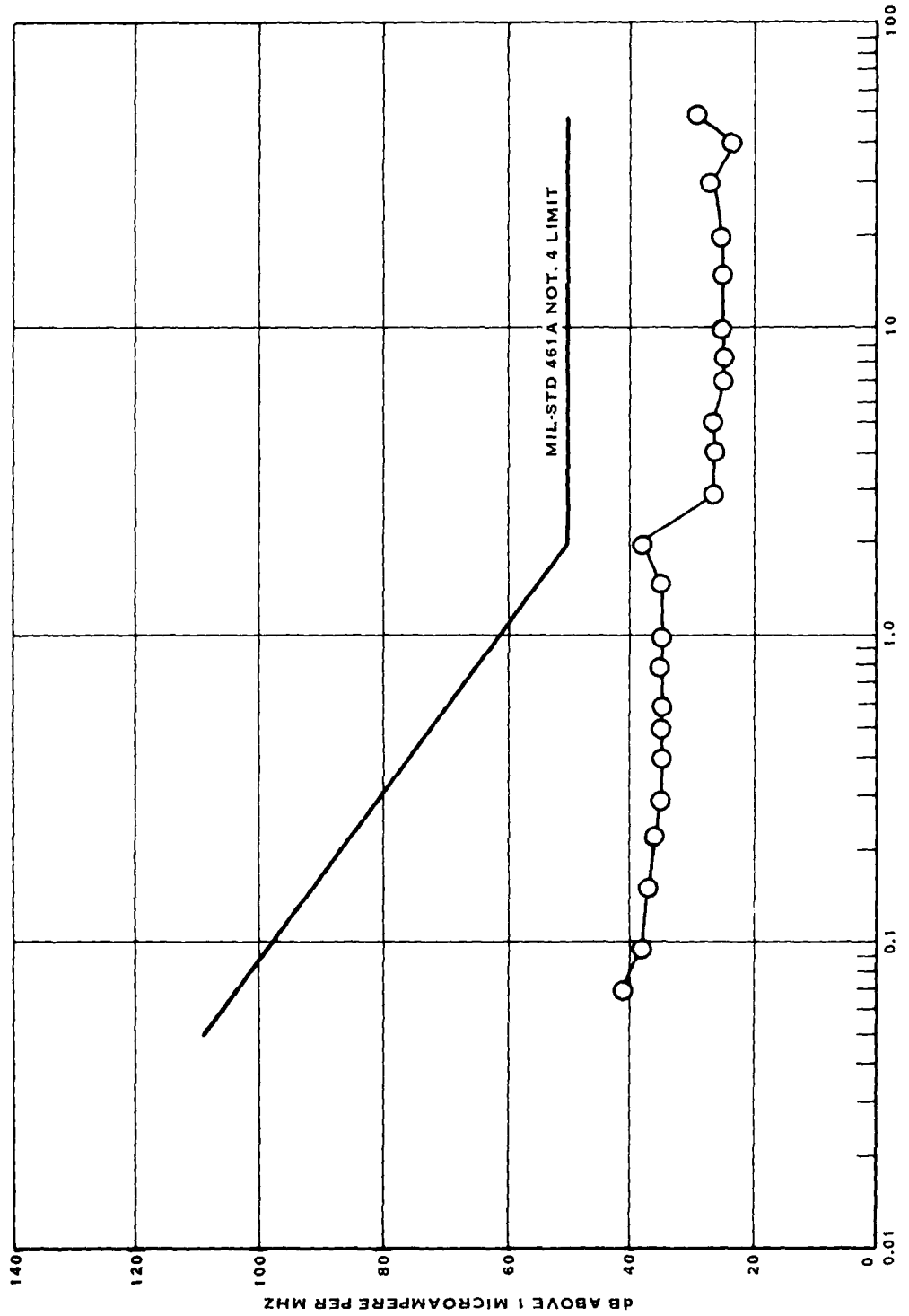


FIGURE 33. BROAD-BAND CONDUCTED EMISSIONS ON THE AIRS 24 VDC POWER RETURN (CE04 TEST)

TABLE 22. AIRS CRASH SURVIVABLE MEMORY MODULE (CSMM)
SURVIVABILITY TEST REQUIREMENTS PER TSO-C51a

These environments shall be imposed on a single sample and in the order specified.

Humidity:	Exposure for ten 24-hour humidity cycles at 95 to 100 percent relative humidity over a temperature range of 38°C to 70°C.
Impact:	The sample shall be exposed to six shocks along each of the three main orthogonal axes. The applied shocks shall be half-sine, 1000g peak with a 5 millisecond duration.
Penetration:	The sample shall be struck once on each side in the most critical plane with a 500-pound steel bar dropped from a height of 10 feet. The point of contact shall be no more than 0.05 square inch. The longitudinal axis of the bar is to be vertical at the moment of impact.
Static Crush:	A force of 5000 pounds shall be applied for 5 minutes to each of the sample's three main orthogonal axes (one axis at a time).
Fire Protection:	The sample shall be exposed to flames of 1100°C enveloping at least half of the outside area for a period of at least 30 minutes.
Water Protection:	The sample shall be immersed in salt water to a depth of 6 feet for at least 36 hours.

Conventional design techniques were applied to the humidity, impact shock, static crush, and water immersion environments. The unique environments of penetration and flame exposure required a series of material and configuration studies and associated development testing to verify the design concepts. The studies and development tests led to a CSMM configuration which satisfied the requirements for the AIRS application.

The CSMM employs a water boil-off technique for heat dissipation to meet the flame exposure requirement of TSO-C51a. Because of this water contained in the CSMM, the TSO-C51a humidity exposure tests would be superfluous and were therefore not performed.

Test Results

The test items performed acceptably throughout the initial survivability test and the survivability retest with the exception of one undesirable effect which occurred during the initial flame test. The undesirable effect was the melting of the aluminum housing from direct flame exposure due to the severe corner splitting of the intumescent material. The severe corner splitting was due to a thin aluminum coating over the intumescent material which restricted uniform intumescence. Approximately 60 percent of the aluminum housing had melted by the conclusion of the initial flame test. See Table 23 for the results of all the survivability tests.

After disassembly of the CSMM, it was determined that the materials which comprise the boiler layers protected the memory device from the direct flame. See Figure 34 for the test facility setup. The inner two boiler layers were still moist, indicating that the temperature of the memory device did not exceed 100°C. The disassembled CSMM is shown in Figures 35 and 36.

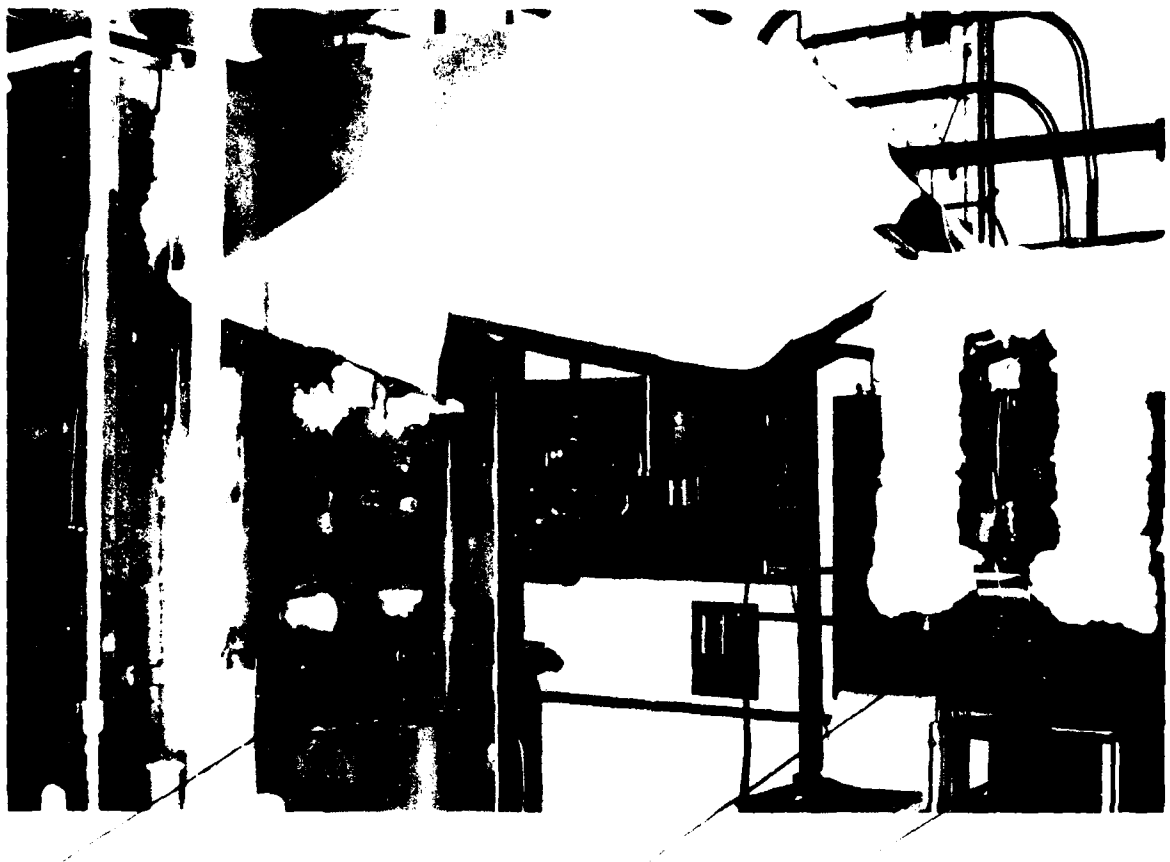
Development tests with the intumescent material were performed by Hamilton Standard and the 3M Corporation located in St. Paul, Minnesota. The method which proved to minimize the corner splitting was a shell molded from the intumescent material reinforced by an inner layer of wire mesh. The redesigned intumescent coating and a development test sample which used the redesigned coating are shown in Figure 37. The CSMM successfully passed a complete survivability retest with no adverse effects using the redesigned coating. Figure 38 shows the CSMM following the second flame test.

Computer comparison of the presurvivability test data and the post survivability test data proved that no data was lost as a result of the survivability test or retest programs. The presurvivability test data stored included a random pattern of information filling all memory locations. No data bits were lost or changed as a result of the survivability test environments.

Hamilton Standard has concluded that the ability of the AIRS CSMM to protect a solid-state memory device in an aircraft crash environment has been successfully demonstrated.

TABLE 23. AIRS CSMM SURVIVABILITY TEST CHRONOLOGY

DATE	TEST PERFORMED	GOVERNMENT SPECIFICATION	RESULT	NOTES
10/15/79	Functional	N/A	Passed	
10/16/79	Impact Shock	FAR 37.150, TSO-C51a Para. 7.8.2, Type I	Passed	Post impact shock data verification could not be performed
10/19/79 and 10/23/79	Penetration	FAR 37.150, TSO-C51a Para. 7.8.3, Type	Passed	Weight of test block was erroneously measured (see Penetration tester, Figure 39).
10/22/79	Static Crush	FAR 37.150, TSO-C51a Para. 7.8.4, Type I	Passed	
10/24/79	Flame	FAR 37.150, TSO-C51a Para. 7.8.5, Type I	Passed	Intumescent coating split causing aluminum housing to melt
10/29/79 to 10/31/79	Sea Water Immersion	FAR 37.150, TSO-C51a Para. 7.8.6	Passed	No data was lost as a result of the survivability tests
11/30/79	Functional (Retest)	N/A	Passed	
12/3/79	Impact Shock (Retest)	FAR 37.150, TSO-C51a Para. 7.8.2, Type I	Passed	
12/5/79	Penetration (Retest)	FAR 37.150, TSO-C51a Para. 7.8.3, Type I	Passed	The flex tape was sheared off
12/7/79	Static Crush (Retest)	FAR 37.150, TSO-C51a Para. 7.8.4, Type I	Passed	
12/10/79	Flame (Retest)	FAR 37.150, TSO-C51a Para. 7.8.5, Type I	Passed	
12/12/79 to 12/14/79	Sea Water Immersion (Retest)	FAR 37.150, TSO-C51a Para. 7.8.6	Passed	No data was lost as a result of the survivability retest



AVCO 3 D SUBSCALE
FIRE SIMULATION
TEST FURNACE

DIGITAL RECORDER

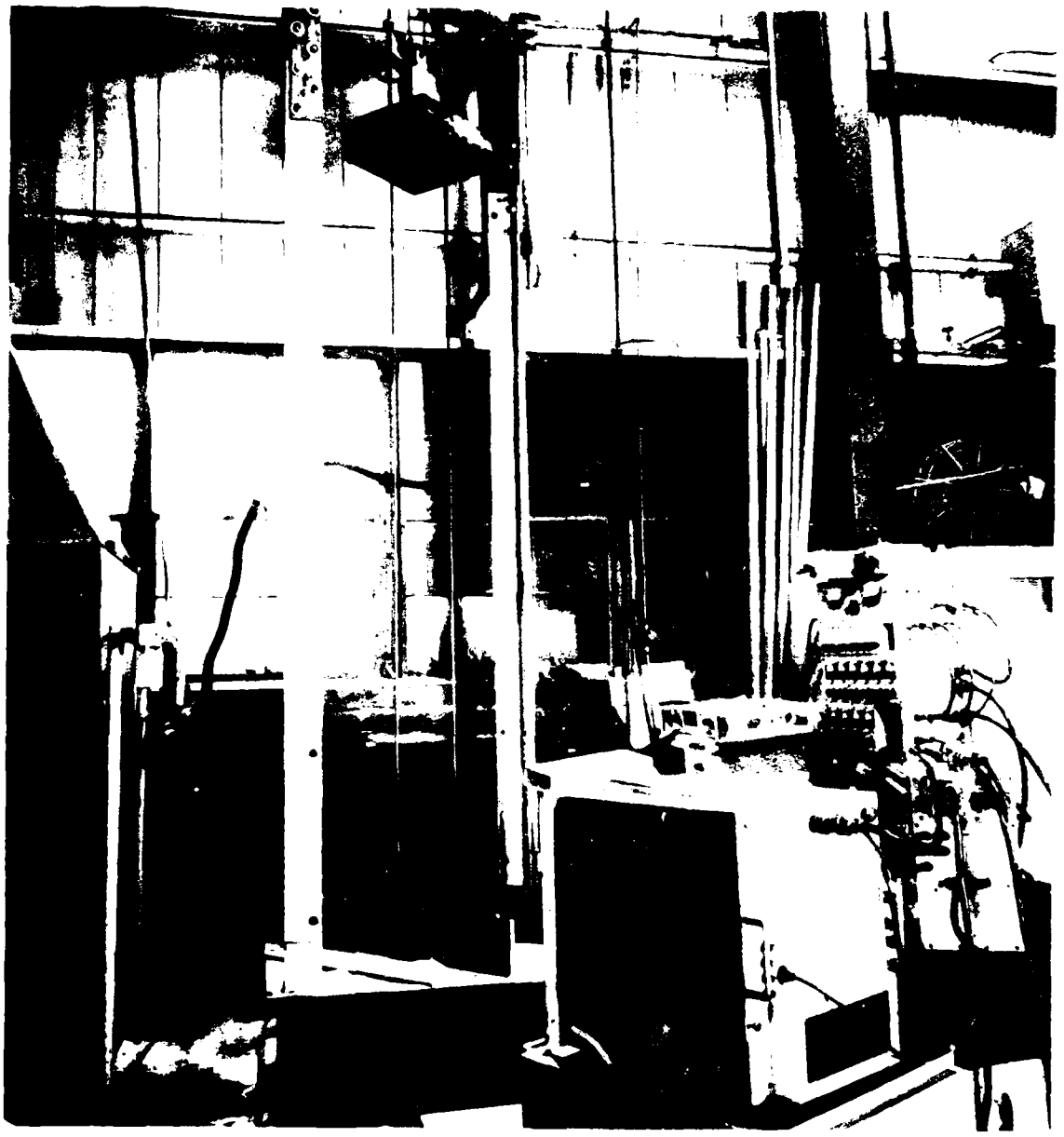
AIRS MODULE ASSY
UNC DATED

1100°C CHAMBER TEMP
17.5 BTU FT^{-2} SEC RADIATIVE HEAT FLUX
.5 BTU FT^{-2} SEC CONVECTIVE HEAT FLUX

[illegible]

FIGURE 35. FIRST CSMM FLAME TEST - UNIT DISASSEMBLED

FIGURE 88. [illegible]



IMPACT ACCELEROMETER TESTS

Two commercially available accelerometers were procured for characterization and AIRS impact acceleration data gathering tests. These tests evaluated the accelerometers for applicable use in measuring crash impact accelerations for the AIRS. The accelerometers were subjected to functional characterization at ambient, high (160°F), and low (-65°F) temperatures and were then subjected to simulated crash impact shocks at the Acton Laboratories in Acton, Massachusetts. The accelerometer outputs were simultaneously recorded by a recording oscillograph and the AIRS.

The two accelerometers tested were:

1) Humphrey, Inc. ±150g Linear Accelerometer P/N LA45-0122-1
2) Edcliff Instruments ±150g Subminiature Accelerometer P/N 121992-4

Functional Tests

1) Power Dissipation

   Power dissipation did not exceed 100 milliwatts.

2) Static Error

   The maximum static error band tested at each 10% of range was within ±1.5% of full scale.

3) Linearity

   Linearity determined from the static error tests did not exceed ±1%.

4) Hysteresis

   Tested with a continuously applied 0g to ± full scale and back to 0g acceleration. The test item did not exceed 0.6% hysteresis band.

5) Resolution

   Tested at 25%, 50%, and 75% of full scale, the resolution was within 0.5% of full scale or better.

6) Crosstalk

   Response to full scale accelerations applied normal to the sensitive axis did not exceed 0.01g/g.

7) Damping Factor

   The frequency response of the test items did not exceed the following limits over the full operational temperature range:

   a) Edcliff accelerometer: 0.4 to 1.1
   b) Humphrey accelerometer: 0.3 to 0.6

Environmental Tests

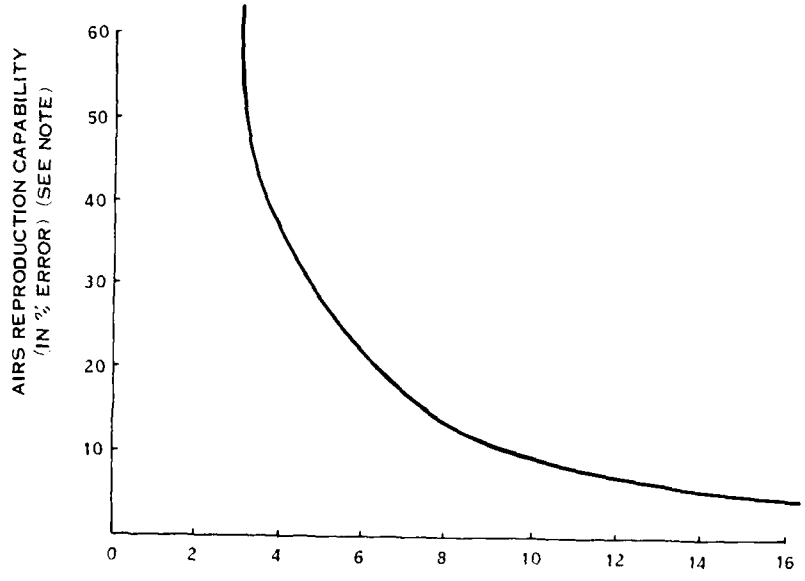
1) Temperature

The test items were subjected to temperature cycling tests in accordance with MIL-STD-810B, Method 503. The test items were operated as in the static error, hysteresis, and damping factor tests during the temperature cycling and met the manufacturers' specifications.

2) Shock

The test items were subjected to a shock spectrum simulating (as near as practicable) an aircraft crash environment. The shock impulses were simultaneously monitored by test reference instrumentation and the AIRS.

Comparison of shock results verified adequate reproduction of the shock waveform utilizing the AIRS recorded data. Correlation of the AIRS waveform reconstruction with the instrumentation data was determined by comparison of the areas under the curve. The correlation was within the tolerance limits shown in Figure 40.



NOTE: THE % ERROR REPRESENTS EXPECTED ERROR FACTOR IN REPRODUCING AREA UNDER CURVE OF THE SHOCK IMPULSE VIA GROUND SOFTWARE TECHNIQUES.

FIGURE 40. EXPECTED "G" INPUT REPRODUCIBILITY

Test Results

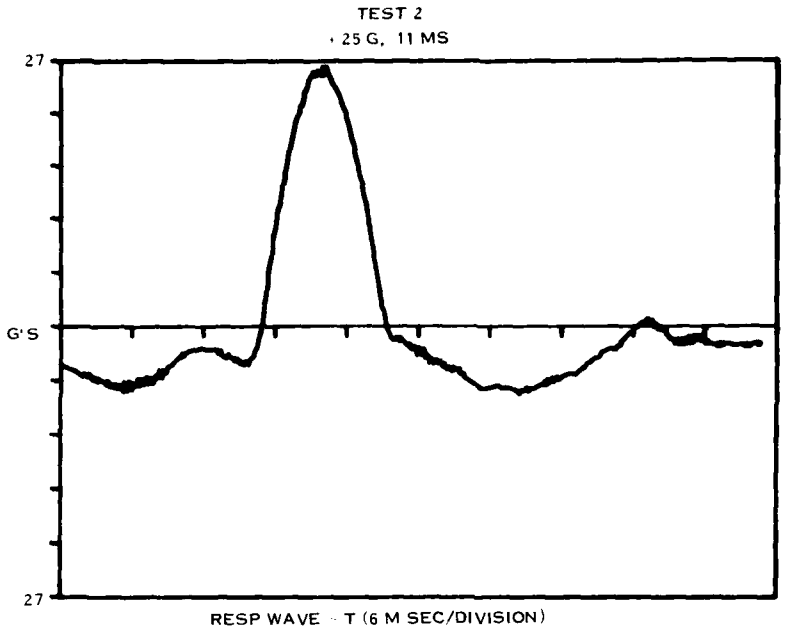
The two accelerometers tested performed within manufacturers' specifications throughout the test program. The two test items did demonstrate different dynamic characteristics. The Edcliff unit was slightly slower to respond and demonstrated some overshoot during the 25G, 11-millisecond tests. Therefore, the Humphrey unit appeared to be better suited to the AIRS application although either would perform acceptably.

Table 24 shows the results of the AIRS Impact Accelerometer Tests.

Figure 41 shows in graphic form the data obtained during the shock tests.

TABLE 24. AIRS IMPACT ACCELEROMETER TEST CHRONOLOGY

DATE	TEST PERFOMED	RESULTS	REMARKS
TEST ITEM: HUMPHREY INC. ±150 G LINEAR ACCELEROMETER P/N LA45-0122-1 S/N H1			
24 Sept 79	Power Dissipation	Passed	
24, 26 Sept 79	Static Error (Accuracy)	Passed	
24, 26 Sept 79	Linearity	Passed	
24, 26 Sept 79	Hysteresis	Passed	
24 Sept 79	Resolution	Passed	
24, 26 Sept 79	Repeatability		No requirement specified
26 Sept 79	Crosstalk	Passed	
26 Sept 79	Damping Factor	Passed	
24, 26 Sept 79	Temperature	Passed	
3 Jan 80	Shock	Passed	
TEST ITEM: EDCLIFF INSTRUMENTS ±150 G SUBMINIATURE ACCELEROMETER P/N 121992-4 S/N 2902			
20 Sep 79	Power Dissipation	Passed	
20, 26 Sept 79	Static Error (Accuracy)	Passed	
20, 26 Sept 79	Linearity	Passed	
20, 26 Sept 79	Hysteresis	Passed	
20, 26 Sept 79	Resolution	Passed	
20,26,27 Sept 79	Repeatability		Met Manufacturer's Specification
20 Sept 79	Crosstalk	Passed	
26 Sept 79	Damping Factor	Passed	
20,26,27 Sept 79	Temperature	Passed	
3 Jan 80	Shock	Passed	



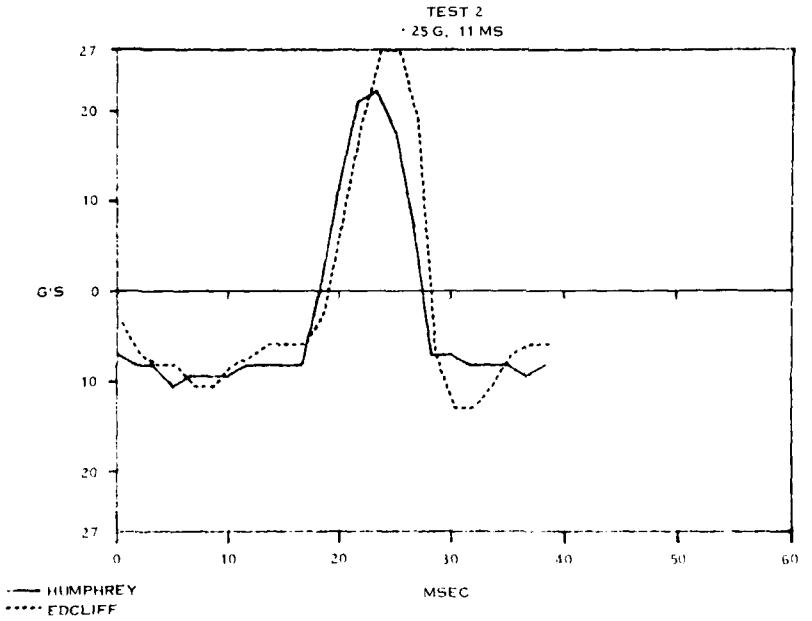
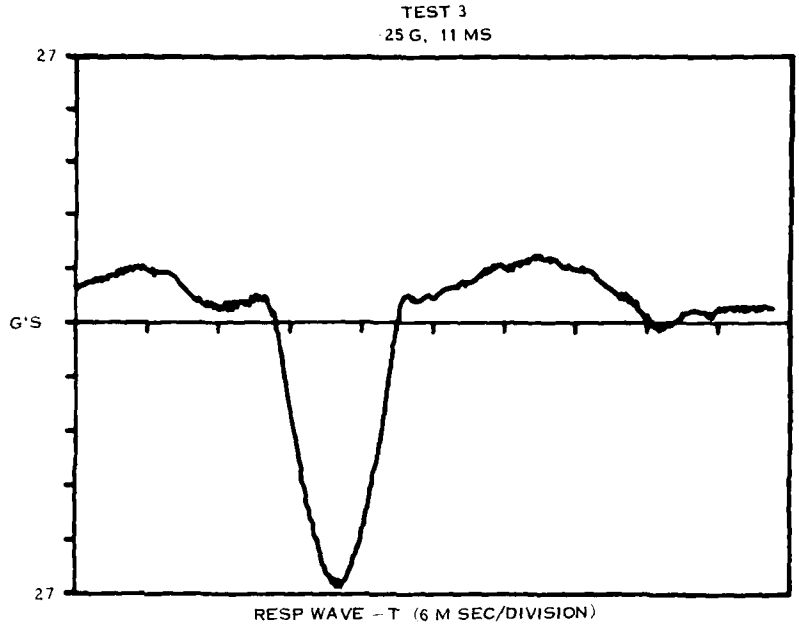


FIGURE 41. AIRS IMPACT ACCELEROMETER SHOCK TEST



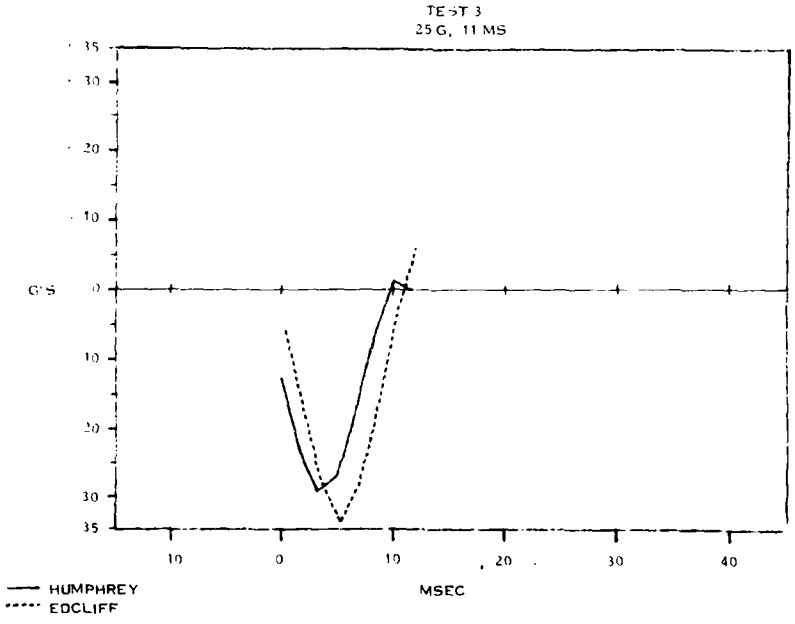
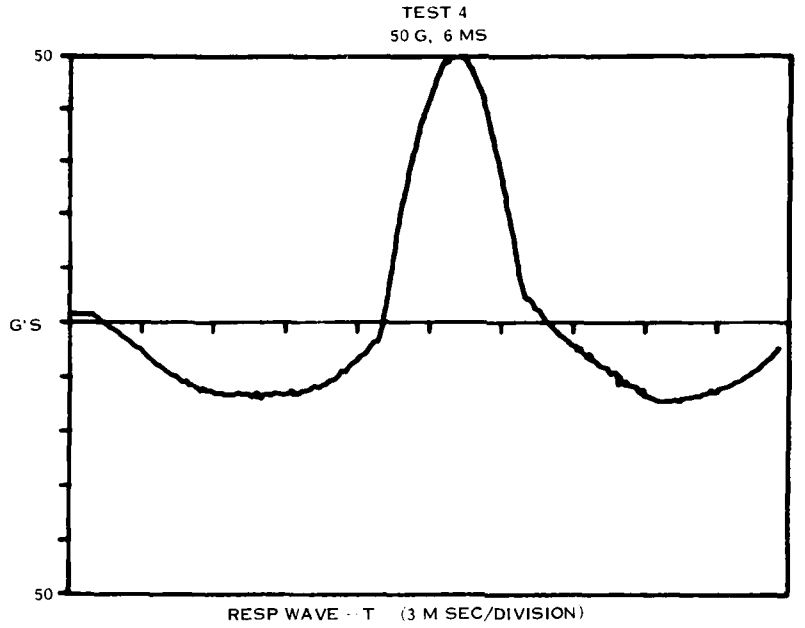


FIGURE 41. AIRS IMPACT ACCELEROMETER SHOCK TEST (CONTINUED)



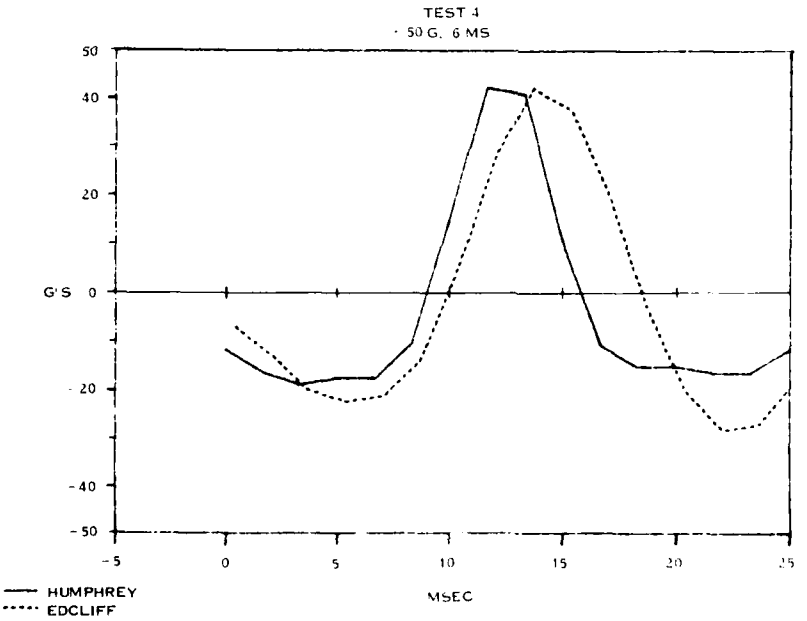


FIGURE 41. AIRS IMPACT ACCELEROMETER SHOCK TEST (CONTINUED)

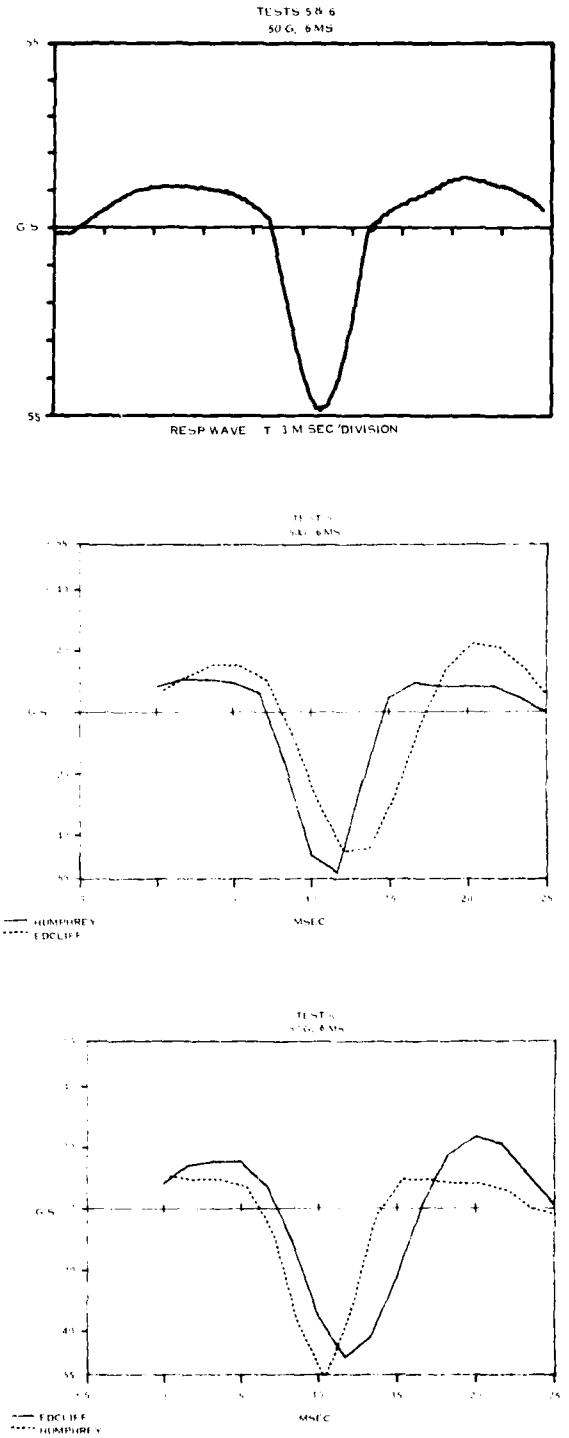


FIGURE 41. AIRS IMPACT ACCELEROMETER SHOCK TEST (CONCLUDED)

PHASE III FLIGHT TEST

The flight testing of the AIRS brassborad electronics unit was accomplished in three segments due to the availability of the helicopter. The flight tests took place in February, July, and November of 1980, accumulating a total of 6.8 test hours.

The AIRS brassboard electronics unit used during flight test is functionally equivalent to the production configuration except for the following added capabilities:

* The AIRS brassboard allows interfacing with the Westinghouse BORAM system in addition to the Hamilton Standard developed hybrid memory.

* Added program and scratch-pad memory was added to allow greater software capability for development testing and software debugging.

* The CSMM was not part of the brassboard; instead, the memory device was mounted directly on the Memory Control card.

* A digital flight data Quick Access Recorder (QAR) interface was provided for recording the continuously sampled AIRS data to provide a baseline against which to compare the reconstructed memory device compressed data.

The AIRS flight test airborne system differed from the production concept in several areas. The flight test configuration did not record stabilator position, ice rate, aircraft discretes, or impact accelerations because these parameters were either unavailable or impractical to record. The signal source for several parameters that were recorded differed from the production source. These parameters included airspeed, vertical velocity (altitude rate), and control positions. These differences were expected to have a negligible impact on the flight test results.

The flight test configuration used eight of the AIRS discrete input channels to record Sikorsky's Real Time Acquisition and Processing of Inflight Data (RAPID) system run numbers for correlation of the AIRS data to the Sikorsky data.

For the flight test program, the AIRS sampled data was continuously recorded on a digital flight data Quick Access Recorder (QAR) to provide a comparative reference for evaluating the reconstruction of the AIRS compressed data. This also provided the ability to evaluate revised data storage and reconstruction algorithms by using QAR data in ground computer analysis.

The AIRS brassboard electronics unit measured 8.0 inches high by 10.25 inches deep by 10.0 inches wide and weighed approximately 15.0 pounds. The QAR measured 7.75 inches high by 19.75 inches deep by 5.0 inches wide and weighed approximately 19.0 pounds.

The AIRS installed on the BLACK HAWK (UH-60A) helicopter tail number 77-22714 consisted of the AIRS brassboard electronics unit and the Digital Flight Data Recorder (QAR). The AIRS unit interfaced to various aircraft and instrumentation signals.

The AIRS installation was tested prior to flight test via a calibration test to verify that aircraft sensors were not adversely affected by the AIRS.

AIRS FLIGHT TEST INSTALLATION

Wiring Installation

The AIRS was installed as an "orange-wire" instrumentation system on the BLACK HAWK helicopter in accordance with Sikorsky Aircraft requirements for installation and wiring of measurement systems in experimental test helicopters. In accordance with these requirements, wiring installation was defined on Development Engineering Orders (DEO's) for interfacing directly to aircraft sensors. In instances where existing instrumentation systems were already installed, an Engineering Work Request (EWR) covered the installation of a parallel instrumentation system.

The initial instrumentation system installed on BLACK HAWK helicopter #AK714 was covered in Sikorsky Engineering Report SER70078[5]. The AIRS paralleled this instrumentation system and conformed to the guidelines specified by Sikorsky Aircraft with respect to minimum load requirements as defined in Table 25. The installation was accomplished via an EWR which defined the wire routing as shown in Figures 42, 43, and 44.

The Heading, Pitch Attitude, and Roll Attitude installation wiring was accomplished via DEO 76308 since no instrumentation system existed for these signals. The Encoding Altimeter connections were accomplished via DEO 76309 since this sensor was not connected to an instrumentation system either. A DEO reference master is shown in Figure 45. Figure 46 shows the actual wiring diagrams for DEO's 76308 and 76309. Table 25 provides the guidelines for the attitude and altimeter sensors specified by Sikorsky Aircraft with respect to minimum load requirements. The load imposed on the aircraft sensors by the AIRS is also included in the table.

5. Sikorsky Engineering Report, SER70078 - UTTAS FLIGHT TEST VEHICLE NOS. 1, 2, AND 3, - AIRBORNE DATA ACQUISITION SYSTEM, Prepared under Contract DAAO01-73-C-0006 (PGA), P00100, 17 November 1978, Sikorsky Aircraft, Stratford, CT.

TABLE 25. AIRS PARAMETER LISTING

Parameter	Data Range	Signal Range	Scaling	Source Impedance In Ohms	Suggested Min Load (In Ohms)	Actual AIRS Load (In Ohms)
Barometric Altitude	-1,000 ft to +50,000 ft	0.5 to 12.5 VDC	HI = 9.0V LO = 2.5V	10K	120K	1 Meg
Heading	0 to 360°	0 to 11.8 VAC, 400 Hz		10	10K	100K
Pitch Attitude	±82°	0 to 11.8 VAC, 400 Hz		-	20K	100K
Roll Attitude	±180°	0 to 11.8 VAC, 400 Hz		-	20K	100K
Engine Torque #1	0 to 150%	0 to 5.277 VDC	35mV = 1%	-	200K	400K
Engine Torque #2	0 to 150%	0 to 5.277 VDC	35mV = 1%	-	200K	400K
Main Rotor Speed	0 to 130%	0 to 14,326 Hz	110.2 Hz = 1%	-	100K	100K
Engine Speed (N_G) #1	0 to 110%	0 to 2,349.3 Hz	21.357 Hz = 1%	-	100K	100K
Engine Speed (N_G) #2	0 to 110%	0 to 2,349.3 Hz	21.357 Hz = 1%	-	100K	100K
Stabilator Position	0 to 100%	0 to -2.5 VDC	25mV/1%	50	10K	100K
Load Factor (Vertical Accel)	-3.5 to +5.5g	±2.5 VDC	1.86 g/V	50	10K	100K
Altitude Rate (Rate of Climb)	±3.000 ft/min	±2.5 VDC	50 mV/ ft/sec	50	10K	100K
Airspeed	0 to 0.96 psid	0 to 3.3 VDC	3.33 VDC = 1 PSID	10	10K	100K
Long Stk Pos	0 to 100%	0 to -2.5 VDC	25mV/1%	50	10K	100K
Lat Stk Pos	0 to 100%	0 to -2.5 VDC	25mV/1%	50	10K	100K
Coll Stk Pos	0 to 100%	0 to -2.5 VDC	25mV/1%	50	10K	100K
Pedal Position	0 to 100%	0 to -2.5 VDC	25mV/1%	50	10K	100K

9
B

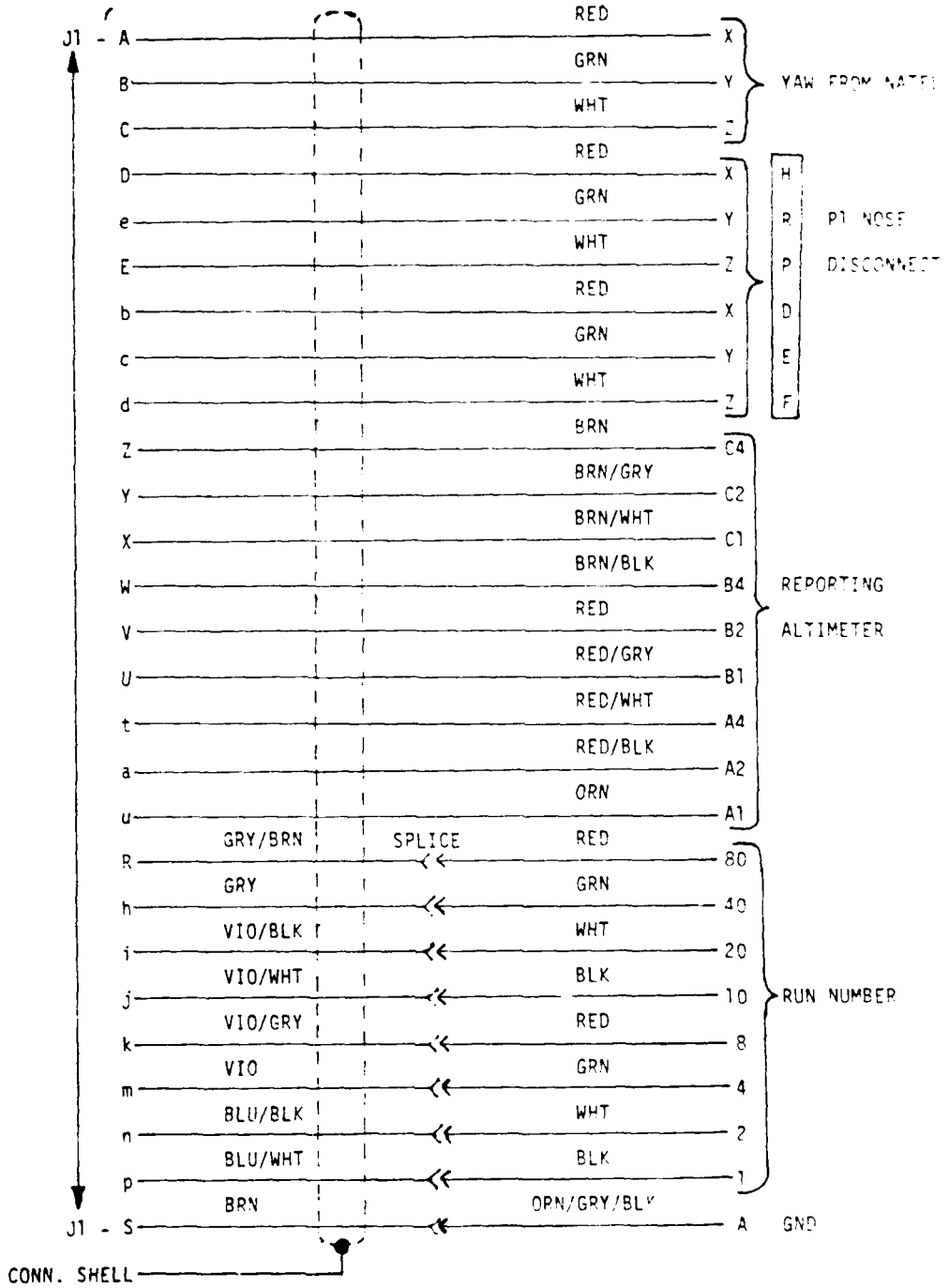


FIGURE 42. AIRS J1 SIGNAL CONNECTOR WIRING

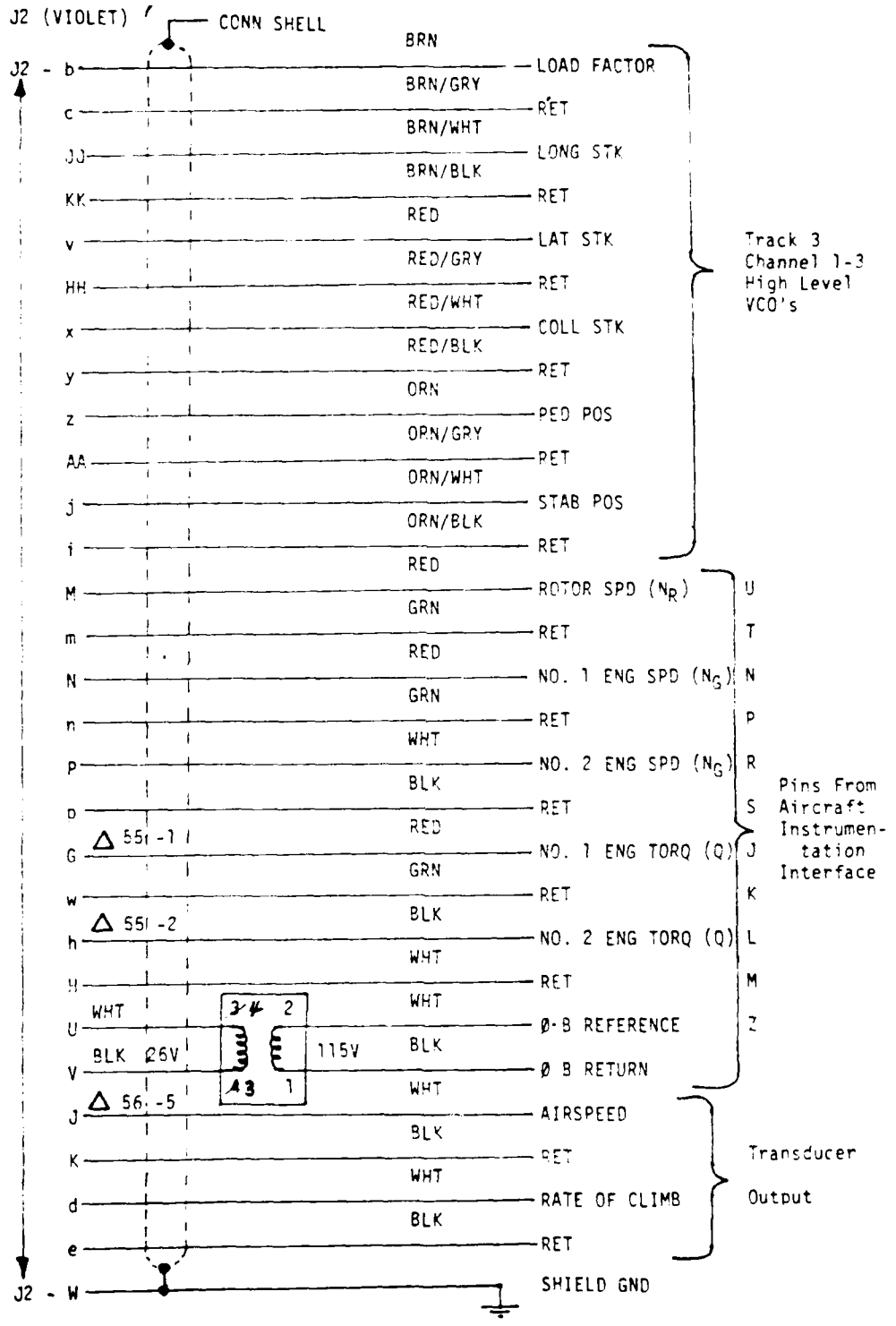


FIGURE 43. AIRS J2 SIGNAL CONNECTOR WIRING

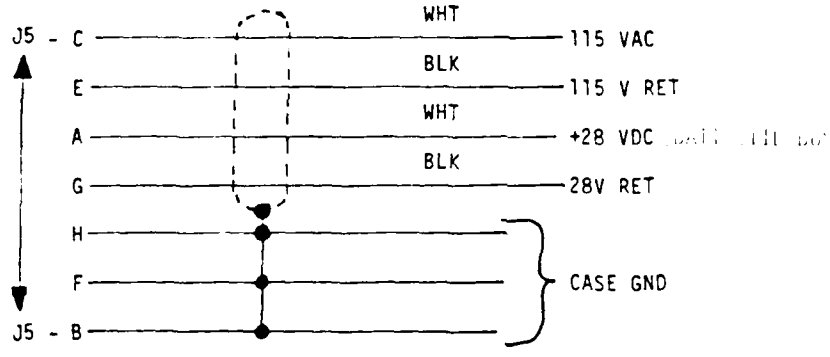


FIGURE 44. AIRS J5 POWER CONNECTOR WIRING

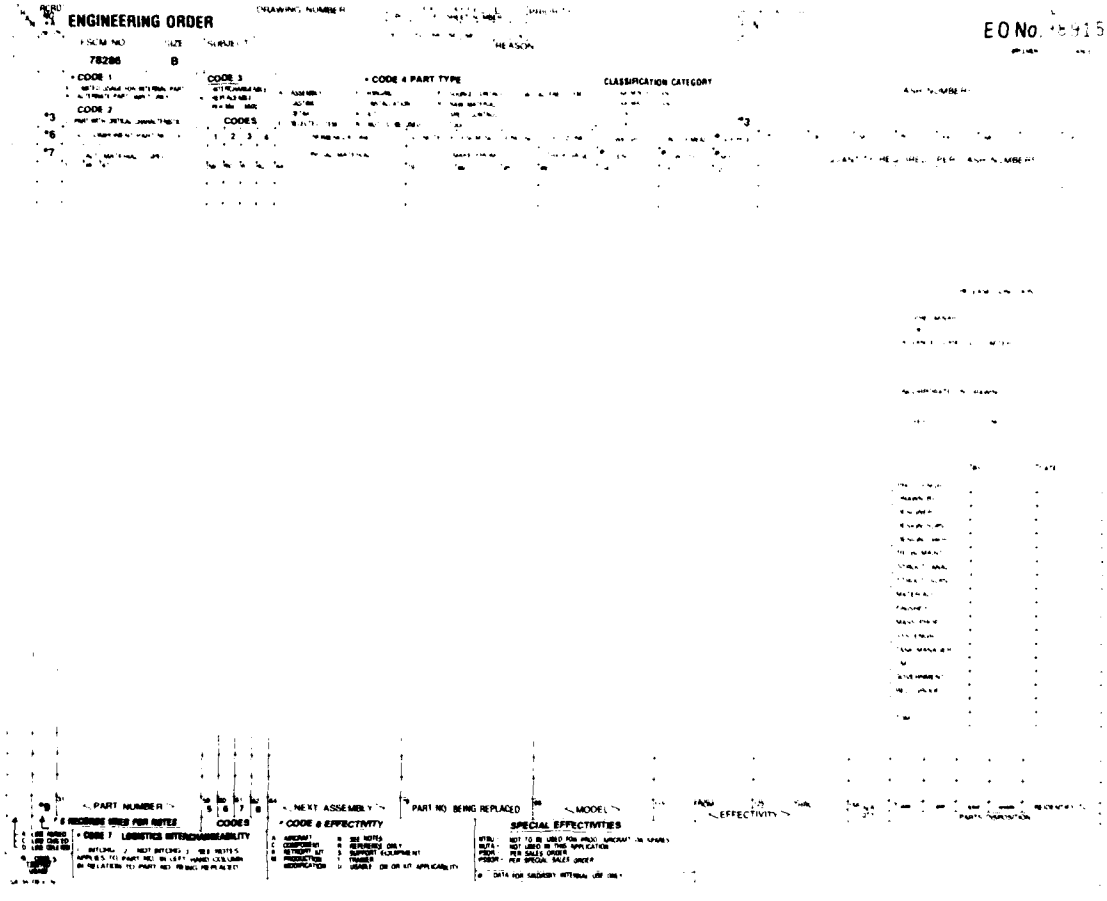


FIGURE 45. DEO REFERENCE MASTER

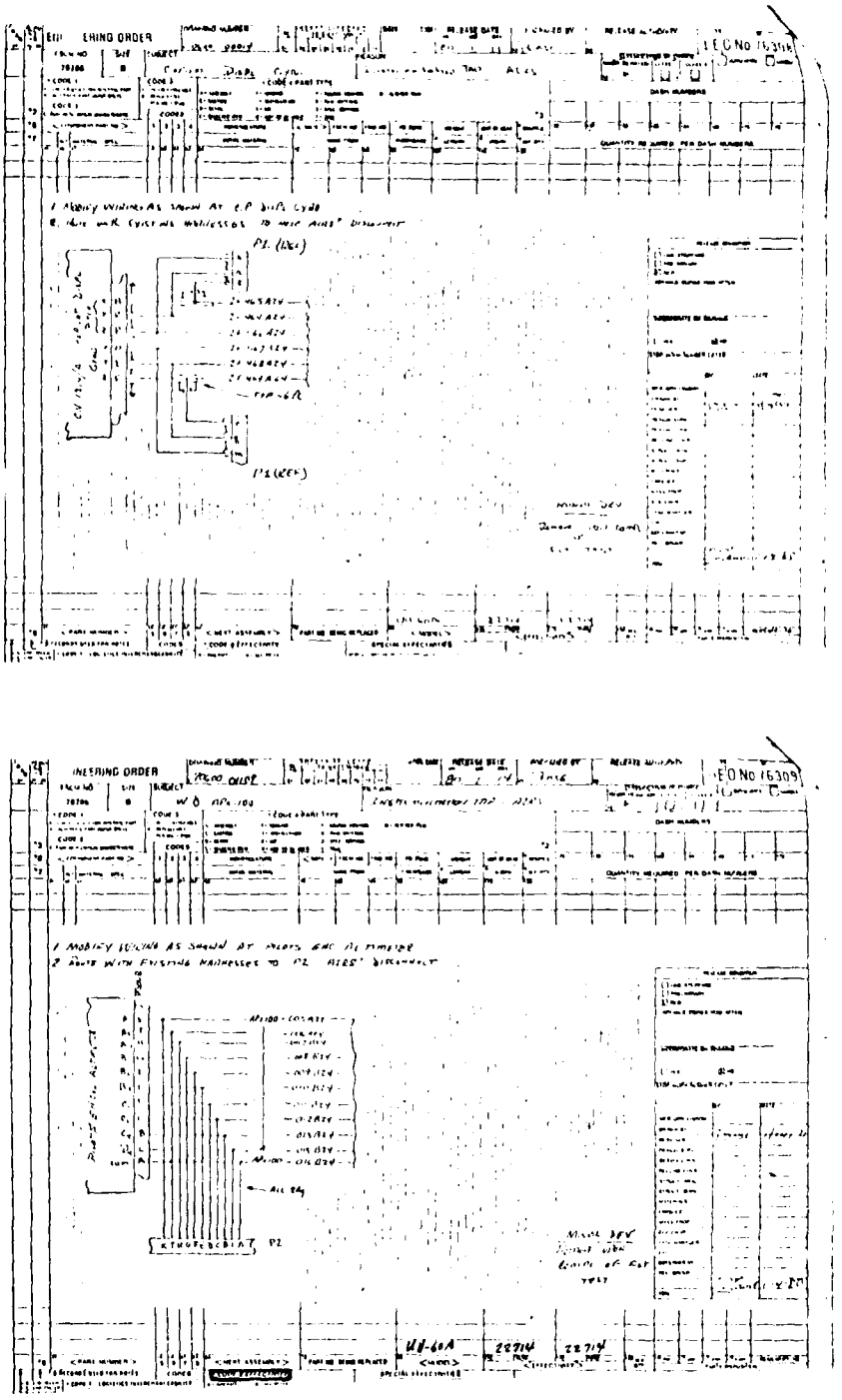


FIGURE 46. DEO'S 76308 and 76309 WIRING DEFINITIONS

Mounting Installation

The AIRS Electronics Unit and the Quick Access, Recorder (QAR) were mounted to a steel plate which was defined by Sikorsky drawing #77-95-01201. Tie-down rings mounted to the bottom of the plate allowed ease of installation in and removal from the helicopter. The AIRS was mounted between Stations 379-395 (see Figures 47) on Butt Line 2.000-18.000 and on Water Line 206.83.

Safety of Flight Review

Following installation of AIRS on the BLACK HAWK, gound tests were performed to verify AIRS compatibility with existing aircraft instrumentation. Signal levels were measured with AIRS connected and disconnected to verify that no adverse effects were introduced into the aircraft system as a result of the AIRS. No adverse effects were evident.

The AIRS was installed in an area in which ballast was normally installed. Ballast requirements for BLACK HAWK flight were coniderably in excess of AIRS weight and was thus not considered a safety of flight factor.

All factors were reviewed by the BLACK HAWK flight control personnel prior to each flight, as a matter of standard operating procedure, and the AIRS was found to be acceptable from a safety of flight standpoint.

FLIGHT TEST

The flight testing was accomplished in three segments due to the "piggy-back" nature of the tests.

During February, the AIRS brassboard installation in the aircraft was checked out. Problems with the aircraft wiring and AIRS interfacing were resolved at this time. The preliminary test indicated two problems that resulted in little useful correlation of AIRS, QAR, and RAPID data. The problems were the inability to record the RAPID system run number and excessive QAR data loss. The RAPID run number interface was modified for proper operation, and shock mounts were incorporated into the QAR installation to minimize data loss prior to further flights.

During July, Hamilton Standard demonstrated that the AIRS interface created no interference with Sikorsky's on-board instrumentation. This was accomplished through static calibration tests and a ground run. On 15 July 1980, a 0.7 hour flight was accomplished. The aircraft was then down for two days of maintenance. On 18 July 1980, three flights were recorded. These flights were 0.3 hours, 2.1 hours, and 1.2 hours, bringing the total to 4.3 hours. Of this 4.3 hours, approximately 3.3 hours of data was successfully recovered. The data from the 15 July flight was almost entirely lost due to power transient difficulties. The rest of the data loss occurred during the last flight on 18 July where 0.4 hour of data was lost due to a QAR malfunction.

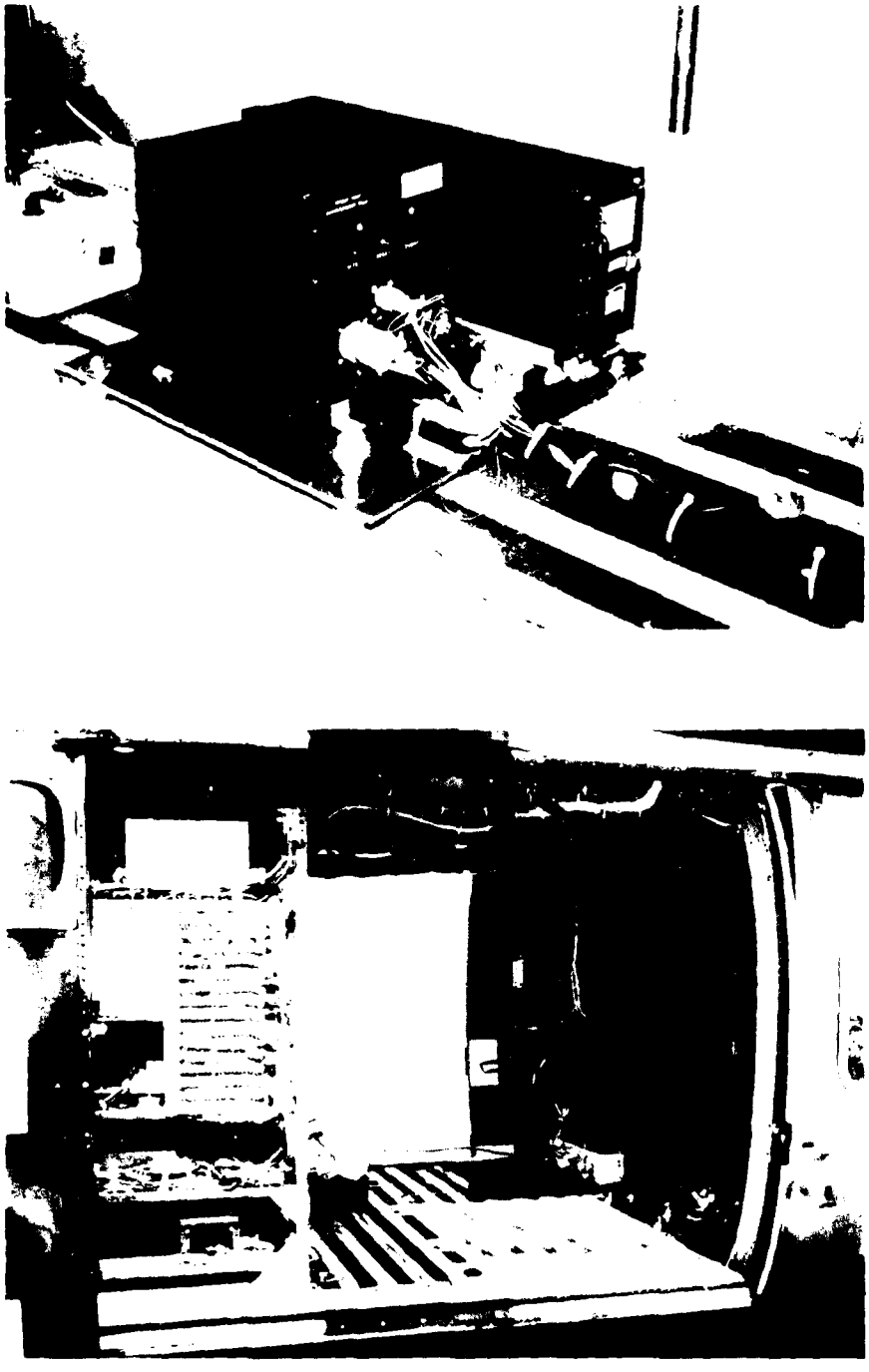


FIGURE 47. AIRS INSTALLATIONS

The AIRS flight test power source was a generator-driven DC bus which is isolated from the aircraft battery during normal operations. When this bus switches from either external power or APU generator power to main generator power, a transient occurs on the bus sufficient to trigger an error in the AIRS.

Analysis of the July flight test resulted in several changes being incorporated prior to further flights. The AIRS power source was changed from the Battery Bus to the Battery Utility Bus. The aircraft battery is directly connected to the Battery Utility Bus at all times, whereas the Battery Bus is connected to the battery via a relay only when no external or generator power is available. This was to eliminate power transients and to more closely simulate the production configuration. The resolutions and floating limits of four parameters were changed to improve data correlation. Airspeed and control positions were recalibrated for the same reason.

Flight testing continued in November 1980 with two test flights and one ground run accomplished. The two flights and the ground run were 0.6 hours, 1.7 hours and 0.2 hours respectively for a total of 2.5 hours. This brought the AIRS flight test program total to 6.8 hours. 5.7 hours of data was recovered for analysis.

The parameters recorded and the final resolutions and floating limits used during flight test are shown in Table 26.

The variable data format used is shown in Table 27.

FLIGHT TEST DATA ANALYSIS

Six flights totaling 6.6 hours resulting in 5.5 hours of recovered flight data were accomplished. For this data analysis, only the two longer flights of 18 July 1980 and the two flights of 7 November 1980 totaling 4.4 flight hours were used. This provided 4.0 hours of flight data for analysis.

Airspeed

AIRS compressed data for this parameter tracked the QAR data well. However, during the July flight's the QAR data appeared slightly noisy and the AIRS data and the RAPID data paralleled, but differed in absolute value. This signal was calibrated prior to the November flights. In the November flights, the QAR data showed a more significant amount of noise than in July. This noise was at a very low frequency, approximately 1/4 Hz, and had enough amplitude to have a significant effect on the AIRS data compression. The noise decreased data compression by effectively decreasing the floating limit by the amplitude of the noise.

The AIRS, QAR, and RAPID data correlated well except for the noise.

The flight test configuration used an instrumentation sensor with characteristics significantly different from the production sensor. For this reason, the

TABLE 26. AIRS FLIGHT TEST PARAMETER LIST

ANALOG	DATA RANGE	SIGNAL RANGE	RESOLUTION	LIMIT EXCEEDANCE
Airspeed	0 to 200 k	0 to +3.3V	--	--
Altitude Rate	±3000 fpm	±2.5V	24 fpm	94 fpm
Load Factor	-3.5 to +5.5 g	±2.5V	0.14 g	0.28 g
Torque-Engine 1	0 to 150%	0 to +5.277V	2.23%	4.46%
Torque-Engine 2	0 to 150%	0 to +5.277V	2.23%	4.46%
Collective	0 to 100%	0 to -2.5V	3.2%	6.4%
Cyclic-Lateral	0 to 100%	0 to -2.5V	1.6%	3.2%
Cyclic-Longitudinal	0 to 100%	0 to -2.5V	1.6%	3.2%
Rudder Pedals	0 to 100%	0 to -2.5V	1.6%	3.2%
Frequency				
RPM-Rotor	0 to 130%	0 to 14,326 Hz	2%	4% @ 100%
RPM-Engine 1	0 to 110%	0 to 2349.3 Hz	1.5%	3.0% @ 100%
RPM-Engine 2	0 to 110%	0 to 2349.3 Hz	0.38%	0.76% @ 50%
Synchro				
Heading	0 to 360°	0 to 11.8 VAC	1.8°	1.8°
Roll Attitude	±180°	0 to 11.8 VAC	0.9°	1.8°
Pitch Attitude	±82°	0 to 11.8 VAC	0.9°	1.8°
Discretes				
Altitude	-100 to 30,000 ft	Low 2.5V High 9.0V	Any Change	Any Change
Rapid Run Number	0 to 99 BCD	TTL	Any Change	Any Change

TABLE 27. FLIGHT TEST VARIABLE DATA FORMAT

BIT POSITION	DATA	
N	SIGNAL IDENTIFICATION	BIT 5
N + 1	SIGNAL IDENTIFICATION	BIT 4
N + 2	SIGNAL IDENTIFICATION	BIT 3
N + 3	SIGNAL IDENTIFICATION	BIT 2
N + 4	SIGNAL IDENTIFICATION	BIT 1
N + 5	SIGNAL IDENTIFICATION	BIT 0
N + 6	SECONDS	BIT 5
N + 7	SECONDS	BIT 4
N + 8	SECONDS	BIT 3
N + 9	SECONDS	BIT 2
N + 10	SECONDS	BIT 1
N + 11	SECONDS	BIT 0
N + 12	1ST PARAMETER DATA	MSB

ADDITIONAL LINES AS REQUIRED FOR REMAINING DATA

SIGNAL TABLE

PARAMETER	NUMBER OF BITS	DATA BITS	RESOLUTION
AIRSPEED	BITS 10	0 THRU 9	3.04KTS
ENGINE #1 TORQUE	BITS 7	2 THRU 8	2.23 %
ENGINE #2 TORQUE	BITS 7	2 THRU 8	2.23 %
LOADFACTOR	BITS 6	4 THRU 9	0.16 G'S
COLLECTIVE STICK	BITS 5	4 THRU 8	3.2 %
LATERAL STICK	BITS 6	3 THRU 8	1.6 %
LONGITUDINAL STICK	BITS 6	3 THRU 8	1.6 %
PEDAL	BITS 6	3 THRU 8	1.6 %
STABILATOR ACTUATOR #1	BITS 6	4 THRU 9	1.6 %
STABILATOR ACTUATOR #2	BITS 6	4 THRU 9	1.6 %
ALTITUDE RATE	BITS 8	2 THRU 9	46.8 FPM
ICE RATE	BITS 5	3 THRU 7	0.04 GM./CU. METER
ROTOR RPM	BITS 8	4 THRU 11	2% @ 100% RPM
ENGINE #1 RPM (NG)	BITS 8	6 THRU 13	0.38% @ 50% RPM
ENGINE #2 RPM (NG)	BITS 8	6 THRU 13	1.5% @ 100% RPM
HEADING DATA	BITS 8	5 THRU 12	2 DEG.
ROLL DATA	BITS 9	4 THRU 12	1 DEG.
PITCH DATA	BITS 9	4 THRU 12	1 DEG
ALTITUDE	BITS 9	0 THRU 8	100 FEET
SAS WARNING	BITS 1		DISCRETE
SAS/FPS FAULT	BITS 1		DISCRETE
RUN NUMBERS	BITS 8	0 THRU 7	1 COUNT
VERTICAL G'S	BITS 8	2 THRU 9	2.4 G'S
LATERAL G'S	BITS 8	2 THRU 9	2.4 G'S
LONGITUDINAL G'S	BITS 8	2 THRU 9	2.4 G'S

noise on this signal is not considered a problem at this time. In the production configuration, data compression is expected to be better by a factor of from 2 to 3.

Engine Torque

This parameter demonstrated very good correlation between the AIRS, QAR, and RAPID data. No further adjustment of this parameter should be necessary for a production configuration AIRS.

Engine RPM

AIRS and QAR data for this parameter demonstrated excellent correlation. RAPID data was not available for this parameter during the flight test program. No further adjustment of this parameter should be necessary for a production configuration AIRS.

Rotor RPM

For the July flight test, the resolution and floating limit for this parameter was 3.8% and 7.6% respectively at 100% RPM. Within these bounds, the AIRS, QAR, and RAPID data correlate. The resolution and floating limit were changed to 1.9% and 3.8% respectively prior to the November flights. This parameter was also subject to a software fault that resulted in erroneous data after the first memory dump to the QAR. This problem was corrected prior to the November flights.

AIRS, QAR, and RAPID data correlated well in the November flights. The small-resolution and floating limit appears to be the best alternative for the production configuration.

Control Positions

In the July flights, rudder pedal position was unavailable due to aircraft instrumentation problems. Collective and lateral and longitudinal cyclic were recorded. AIRS and QAR data for these parameters correlated adequately for the resolution and floating limit of 3.2% and 6.4% respectively. At these values, the AIRS data reconstructions for cyclic positions were not representative of pilot input because the resolutions and floating limits were larger than normal maneuvering control inputs. The resolution and floating limit on rudder pedal and both cyclic positions were changed to 1.6% and 3.2% respectively for the November flights. The AIRS data paralleled the RAPID data but absolute correlation was difficult to obtain. All control positions were recalibrated prior to the November flights.

In the November flights, the AIRS data reconstructions demonstrated much improved correlation because of the increased resolution. All parameters demonstrated good AIRS, QAR, and RAPID data correlation during these flights. Hamilton Standard recommends the resolution and floating limits of 1.6% and 3.2% respectively for rudder pedal and cyclic positions and 3.2% and 6.4% respectively for collective.

Attitude Parameters

AIRS and QAR data for the heading parameter correlated very well. RAPID data is not available for this parameter. Of the parameters which were working correctly during the flight tests, the heading parameter demonstrated the lowest compression ratio. This, plus the level of data correlation, indicated that the resolution and floating limit of 1.8° for this parameter was excessively small. Hamilton Standard recommends a resolution of 1.8° and a floating limit of 3.6° for this parameter.

The AIRS, QAR, and RAPID data for Roll Attitude and Pitch Attitude demontrated good correlation. However, the ground software data recovery algorithms were incorrectly defined, resulting in shifts in the flight test data.

Vertical Velocity (Altitude Rate)

Vertical velocity (altitude rate) data is unusable in its present state. The signal contains high amplitude (0.3 to 0.4 volts) low frequency (.25 to .3 Hz) noise. This parameter source was a transducer with outputs for altitude and vertical velocity. The vertical velocity was simply the altitude signal differentiated. Sikorsky did not monitor this vertical velocity signal but derived the parameter from the recorded altitude information when necessary. There are two possible conclusions that can be drawn. The first is that this transducer or method of measuring vertical velocity is not adequate. The second is that the data recorded is indicative of the parameter's actual behavior and thus is practically useless. Hamilton Standard feels the transducer used in the production configuration, which uses a different method of measurement, will provide a usable signal. Hamilton Standard also recommends a resolution of 100 fpm and a floating limit of 200 fpm.

Altitude

Altitude was recorded from the transponder mode C output. The resolution and floating limit were 100 feet. Within this tolerance, the AIRS, QAR, and RAPID data correlated well.

Load Factor

Load factor was recorded with a resolution of 0.14g and a floating limit of 0.28g. It has not been recorded or processed with a deadband from 0.5 to 1.5g. This parameter correlated well between AIRS, QAR, and RAPID data.

Data Compression

Data compression ratios for the four analyzed test flights are shown in Table 28.

During the July flights, of the eleven periods recorded, the longest was 16 minutes 59 seconds and the shortest was 8 minutes 12 seconds with an average of 12 minutes 49 seconds. With the elimination of the bad parameters of vertical velocity and rotor rpm, the full memory record time would theoretically

TABLE 28. AIRS FLIGHT TEST COMPRESSION DATA

Flight	1st Flight 18 Jul 80			2nd Flight 18 Jul 80			1st Flight 7 Nov 80			2nd Flight 7 Nov 80		
Flight Time (Hours)	2.1			1.2			0.4			1.7		
AIRS Data Recorded	(H:M:S) 1:44:41			0:36:20			0:23:33			1:19:16		
Compression Ratio(:1)	MAX	MIN	AVERAGE	MAX	MIN	AVERAGE	MAX	MIN	AVERAGE	MAX	MIN	AVERAGE
Airspeed	40.0	8.1	11.6	26.1	9.3	12.8	15.9	3.0	5.6	16.1	2.6	4.7
E1 Torque	26.3	7.3	15.3	13.7	10.3	12.5	5.9	4.1	5.0	17.5	4.3	6.6
E2 Torque	29.4	6.7	16.2	24.7	12.5	13.1	6.2	4.2	5.0	17.5	4.6	6.9
Load Factor	68.4	17.0	40.5	65.4	30.2	46.4	27.4	9.4	13.9	35.0	11.8	20.5
Collective	47.6	17.6	29.2	31.6	20.5	25.6	12.6	7.6	9.5	27.1	7.7	13.8
Lateral Cyclic	62.5	21.4	43.0	57.8	25.6	36.9	9.0	5.9	7.0	23.1	6.5	13.5
Longitudinal Cyclic	52.6	18.9	35.5	39.6	26.1	30.7	7.6	5.1	6.5	19.5	4.0	9.8
Rudder Pedals	-	-	-	-	-	-	18.0	8.5	11.4	40.0	9.9	20.8
Vertical Velocity	3.4	1.4	2.0	2.5	1.7	2.0	1.3	1.3	1.3	1.6	1.2	1.4
RPM-Rotor	56.3	1.7	2.7	58.8	2.6	4.6	46.1	28.7	34.5	64.7	30.0	50.3
RPM-Eng 1	50.0	17.6	32.7	34.2	15.5	25.1	9.2	8.6	9.0	35.0	9.1	16.0
RPM-Eng 2	52.6	21.4	35.5	34.2	17.1	26.3	10.6	8.6	9.4	36.4	9.1	7.1
Heading	10.2	2.4	4.4	5.1	2.4	3.7	4.0	1.8	2.9	8.7	2.5	4.5
Roll Attitude	50.0	2.9	9.3	12.0	7.8	10.2	9.0	2.2	5.4	9.2	3.4	5.0
Pitch Attitude	25.3	5.7	14.5	15.5	12.5	14.4	8.6	4.0	5.2	10.7	4.5	6.6
Altitude	20.0	6.7	10.7	7.8	4.6	5.4	60.3	7.4	19.4	14.5	6.1	9.0
TOTAL	10.7	5.3	8.6	9.7	7.3	8.4	6.7	4.4	5.3	9.3	5.1	6.6
Record Time (M:S)	16:59	8:12	13:05	15:15	8:33	12:06	10:03	6:35	7:51	13:49	6:42	9:54

be 13 minutes 2 seconds for the shortest, 46 minutes 10 seconds for the longest and 27 minutes 31 seconds for the average.

Of the eleven periods recorded during the November flights, the longest was 13 minutes 59 seconds, the shortest was 6 minutes 35 seconds with an average of 9 minutes 20 seconds. The rotor rpm parameter recorded correctly during these flights. Eliminating the bad parameter (vertical velocity), the theoretical record times become 22 minutes 12 seconds for the longest, 8 minutes 25 seconds for the shortest, and 13 minutes 10 seconds average.

For the November flights, the rudder pedal position parameter was added and the resolution and floating limits for rotor rpm and both cyclic positions were changed to half of their value during the July flights.

During flight test, certain parameters were not recorded. These included stabilator position, ice rate of accumulation, and all discretes. Rudder pedal position was not recorded during the July flights. Eight of the discretes were modified and used to record RAPID run numbers to allow time correlation of AIRS and RAPID data. Hamilton Standard estimates that inclusion of the above parameters in the production configuration would reduce data storage times by not more than 5 percent.

The average data compression of all parameters except vertical velocity (altitude rate) and rotor rpm decreased by one-third from 12.5:1 for the July flights to 8.0:1 for November. Part of this is accounted for by the change in the resolutions and floating limits for the two cyclic positions. These parameters collectively decreased by about three quarters from 38.5:1 in July to 9.7:1 in November. Another factor was differences in the flight profile. The flight cards for the flights indicate that the November flights were more active than the July flights. A third factor is the atmospheric conditions. The July flights experienced a small amount of very light turbulence whereas the November flights experienced almost continuous light turbulence.

Airspeed was most affected by the above factors because of the noise on the signal, as was described earlier. The amount of the noise effectively decreases the floating limits. Resolution of the noise problem will significantly increase the data compression on this parameter. The sensor used for this parameter was not the same type as will be used on production aircraft. Altitude and heading were minimally affected by the turbulence although for different reasons. The altitude resolution is 100 feet. This is coarse enough that light turbulence would not have a significant effect. Also, the profile for the November flights did not include as much altitude change as the July flights. On the other hand, for heading, the floating limit of 1.80° is very tight and heading was already very active. Therefore, the increase in activity and turbulence had a minimal effect.

The rest of the parameters were reasonably affected by the turbulence.

The difference between the first and second of the November flights was the flight profile. The first flight was part of a rotor to tail cone clearance test and as a result was a very short, very high activity flight. The second

flight included activities such as climb to altitude, cruise, high speed descent, another cruise, autorotations, and descent to base.

The flight test program identified the areas where refinement was needed. The few areas where refinement is still needed are minor adjustments for which further flight test will not be necessary. These refinements are primarily software in nature. Airspeed will use a different source in the production aircraft, so the noise on the signal now is not indicative of a production system problem.

Data from the second test flight of 7 November 1980 for various parameters is shown in Figures 48 through 53. These figures are representative of the data reconstruction capabilities of the AIRS. The data shown in the figures has been compressed by the AIRS and written into the nonvolatile solid-state memory, then read out from the memory, and reconstructed by ground-based data processing techniques developed by Hamilton Standard.

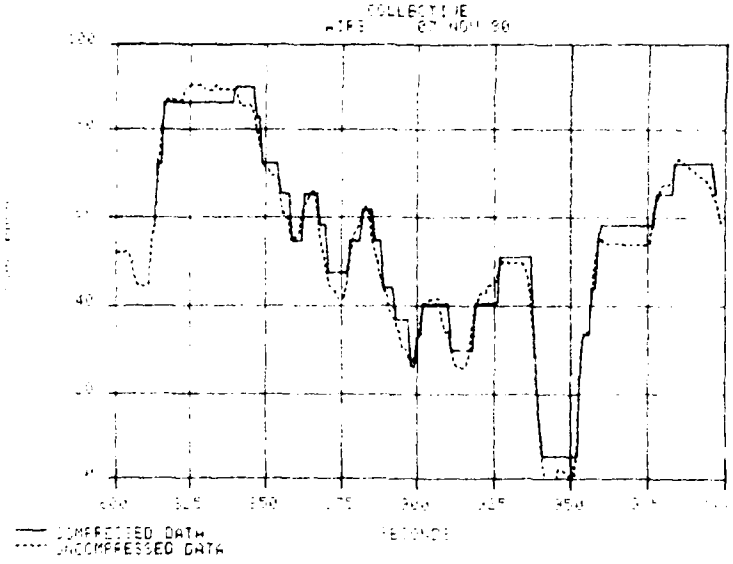


FIGURE 48. AIRS FLIGHT TEST DATA, COLLECTIVE STICK

10
B

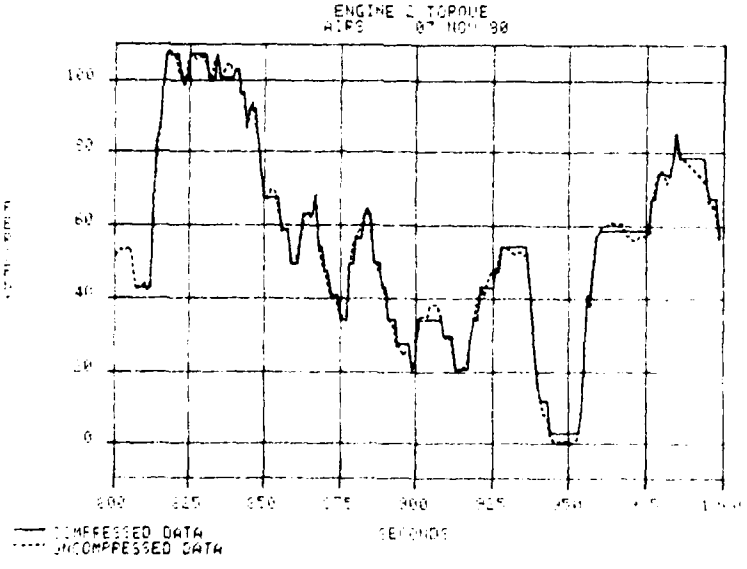


FIGURE 49. AIRS FLIGHT TEST DATA, ENGINE 2 TORQUE

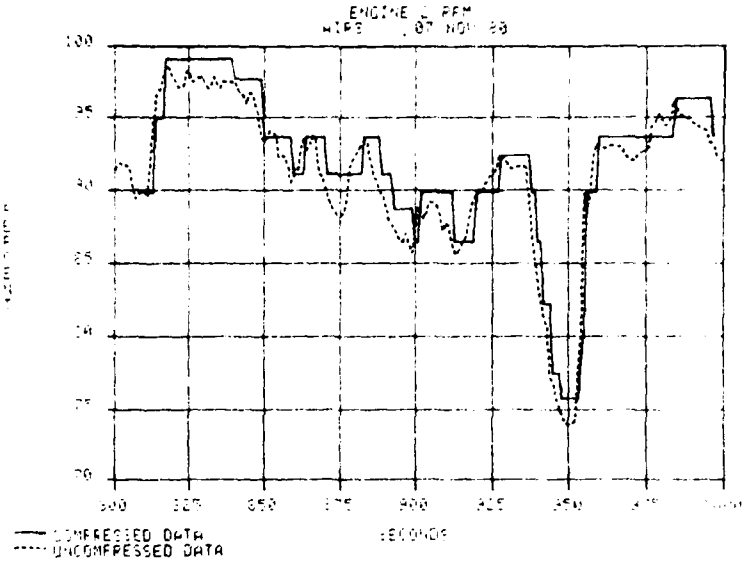


FIGURE 50. AIRS FLIGHT TEST DATA, ENGINE 2 RPM

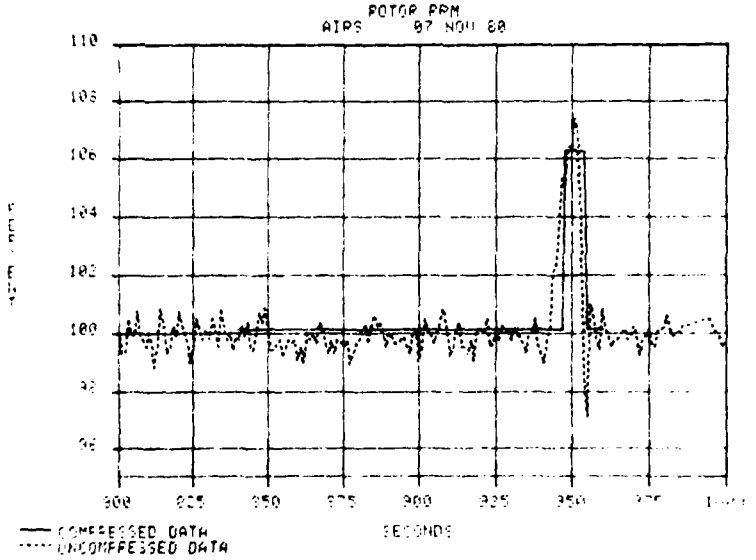


FIGURE 51. AIRS FLIGHT TEST DATA, ROTOR RPM

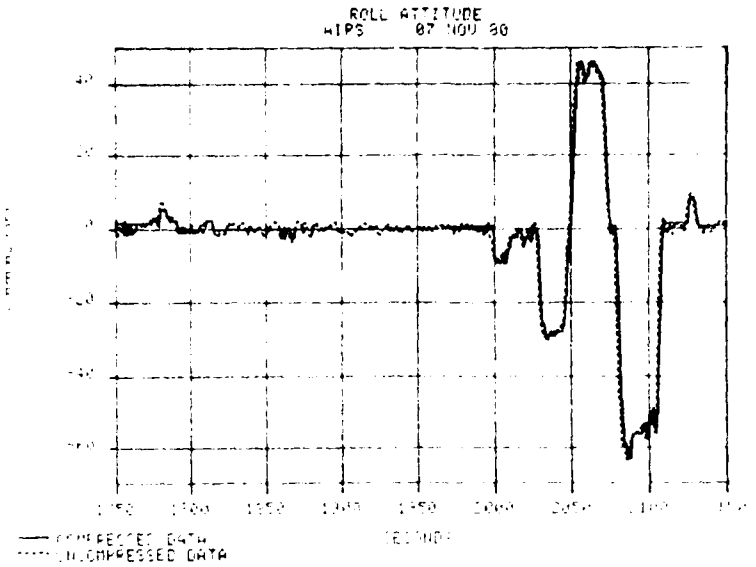


FIGURE 52. AIRS FLIGHT TEST DATA, ROLL ATTITUDE

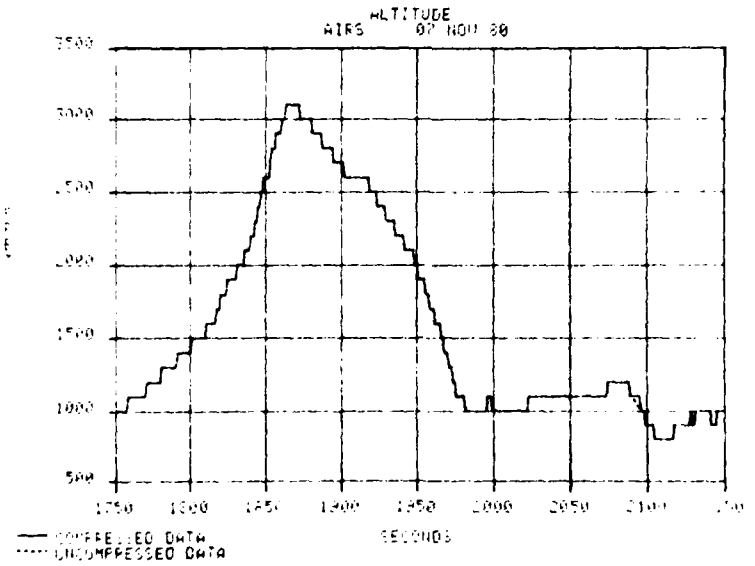


FIGURE 53. AIRS FLIGHT TEST DATA, ALTITUDE

DESIGN ASSESSMENT

The AIRS design as detailed in this report has undergone extensive testing and evaluation. As a result of this effort, Hamilton Standard believes that the basic concept has been proven valid and the majority of the production design details set. The recommendations of this assessment are based on the information gained through the flight tests and other evaluations.

SYSTEMS DESIGN ASSESSMENT

Analysis of the current data storage techniques indicates that approximately 35 to 40% of the memory contains actual data. The other 60 to 65% of memory is taken up by overhead data such as time, data identifiers, and frame identifiers. Changes in data storage formats to those shown in Tables 29, 30, and 31 would result in a decrease in overhead such that the memory would contain about 50% overhead and 50% actual data. This format is such that the percentage of overhead is less dependent on flight activity than the present configuration. This change would increase recording time capability by 25 to 40%.

The primary change in data format is the increase in frame size to 256 bits from 128 bits. With the increase in frame size, the mixed frame is absorbed into the fixed frame and is no longer a separate entity. This change decreases the amount of memory space devoted to frame headers.

The format for the variable data has also been rearranged. Studies indicate that an average of 2.8 to 4.5 floating limit exceedances occurred during the second time periods in which at least one limit exceedance occurred. Current variable data format consists of seconds, parameter identifier, and parameter data for each and every parameter to exceed its limit. The new data format groups all parameter limit exceedance data for any second time frame behind a single header containing seconds and six bits to identify the number of parameters to follow. This format uses less memory space to store the data whenever the number of limit exceedances for any particular 1-second time frame is more than two.

TABLE 29. RECOMMENDED PRODUCTION AIRS FIXED FRAME FORMAT

BIT POSITION	DATA	
0	PROTECT	
1	MINUTES	BIT 7
2	MINUTES	BIT 6
3	MINUTES	BIT 5
4	MINUTES	BIT 4
5	MINUTES	BIT 3
6	MINUTES	BIT 2
7	MINUTES	BIT 1
8	MINUTES	BIT 0
9	FRAME TIME	
10	FRAME TIME	
11	AIRSPEED	BIT 9
12	AIRSPEED	BIT 8
13	AIRSPEED	BIT 7
14	AIRSPEED	BIT 6
15	AIRSPEED	BIT 5
16	AIRSPEED	BIT 4
17	AIRSPEED	BIT 3
18	AIRSPEED	BIT 2
19	AIRSPEED	BIT 1
20	AIRSPEED	BIT 0
21	ENGINE #1 T HOUR	BIT 8
22	ENGINE #1 T HOUR	BIT 7
23	ENGINE #1 T HOUR	BIT 6
24	ENGINE #1 T HOUR	BIT 5
25	ENGINE #2 T HOUR	BIT 4
26	ENGINE #1 T HOUR	BIT 3
27	ENGINE #1 T HOUR	BIT 2
28	ENGINE #2 T HOUR	BIT 8
29	ENGINE #2 T HOUR	BIT 7
30	ENGINE #2 T HOUR	BIT 6
31	ENGINE #2 T HOUR	BIT 5
32	ENGINE #2 T HOUR	BIT 4
33	ENGINE #2 T HOUR	BIT 3
34	ENGINE #2 T HOUR	BIT 2
35	COLLECTIVE	BIT 8
36	COLLECTIVE	BIT 7
37	COLLECTIVE	BIT 6
38	COLLECTIVE	BIT 5
39	COLLECTIVE	BIT 4
40	COLLECTIVE	BIT 3
41	COLLECTIVE STICK	BIT 8
42	COLLECTIVE STICK	BIT 7
43	COLLECTIVE STICK	BIT 6
44	COLLECTIVE STICK	BIT 5
45	COLLECTIVE STICK	BIT 4
46	LATERAL STICK	BIT 8
47	LATERAL STICK	BIT 7
48	LATERAL STICK	BIT 6
49	LATERAL STICK	BIT 5
50	LATERAL STICK	BIT 4
51	LATERAL STICK	BIT 3
52	LONGITUDINAL STICK	BIT 8
53	LONGITUDINAL STICK	BIT 7
54	LONGITUDINAL STICK	BIT 6
55	LONGITUDINAL STICK	BIT 5
56	LONGITUDINAL STICK	BIT 4

BIT POSITION	DATA	
57	LONGITUDINAL STICK	BIT 3
58	PEDAL	BIT 8
59	PEDAL	BIT 7
60	PEDAL	BIT 6
61	PEDAL	BIT 5
62	PEDAL	BIT 4
63	PEDAL	BIT 3
64	STABILATOR ACTUATOR #1	BIT 9
65	STABILATOR ACTUATOR #1	BIT 8
66	STABILATOR ACTUATOR #1	BIT 7
67	STABILATOR ACTUATOR #1	BIT 6
68	STABILATOR ACTUATOR #1	BIT 5
69	STABILATOR ACTUATOR #1	BIT 4
70	STABILATOR ACTUATOR #2	BIT 9
71	STABILATOR ACTUATOR #2	BIT 8
72	STABILATOR ACTUATOR #2	BIT 7
73	STABILATOR ACTUATOR #2	BIT 6
74	STABILATOR ACTUATOR #2	BIT 5
75	STABILATOR ACTUATOR #2	BIT 4
76	ALTITUDE RATE	BIT 9
77	ALTITUDE RATE	BIT 8
78	ALTITUDE RATE	BIT 7
79	ALTITUDE RATE	BIT 6
80	ALTITUDE RATE	BIT 5
81	ALTITUDE RATE	BIT 4
82	ALTITUDE RATE	BIT 3
83	ALTITUDE RATE	BIT 2
84	ICE RATE	BIT 7
85	ICE RATE	BIT 6
86	ICE RATE	BIT 5
87	ICE RATE	BIT 4
88	ICE RATE	BIT 3
89	ROTOR RPM	BIT 11
90	ROTOR RPM	BIT 10
91	ROTOR RPM	BIT 9
92	ROTOR RPM	BIT 8
93	ROTOR RPM	BIT 7
94	ROTOR RPM	BIT 6
95	ROTOR RPM	BIT 5
96	ROTOR RPM	BIT 4
97	ENGINE #1 RPM (N2)	BIT 13
98	ENGINE #1 RPM (N2)	BIT 12
99	ENGINE #1 RPM (N2)	BIT 11
100	ENGINE #1 RPM (N2)	BIT 10
101	ENGINE #1 RPM (N2)	BIT 9
102	ENGINE #1 RPM (N2)	BIT 8
103	ENGINE #1 RPM (N2)	BIT 7
104	ENGINE #1 RPM (N2)	BIT 6
105	ENGINE #2 RPM (N2)	BIT 13
106	ENGINE #2 RPM (N2)	BIT 12
107	ENGINE #2 RPM (N2)	BIT 11
108	ENGINE #2 RPM (N2)	BIT 10
109	ENGINE #2 RPM (N2)	BIT 9
110	ENGINE #2 RPM (N2)	BIT 8
111	ENGINE #2 RPM (N2)	BIT 7
112	ENGINE #2 RPM (N2)	BIT 6
113	HEADING OCTANT	BIT 8

BIT POSITION	DATA	
114	HEADING OCTANT	BIT 7
115	HEADING OCTANT	BIT 6
116	HEADING DATA	BIT 9
117	HEADING DATA	BIT 8
118	HEADING DATA	BIT 7
119	HEADING DATA	BIT 6
120	HEADING DATA	BIT 5
121	ROLL OCTANT	BIT 8
122	ROLL OCTANT	BIT 7
123	ROLL OCTANT	BIT 6
124	ROLL DATA	BIT 9
125	ROLL DATA	BIT 8
126	ROLL DATA	BIT 7
127	ROLL DATA	BIT 6
128	ROLL DATA	BIT 5
129	ROLL DATA	BIT 4
130	PITCH OCTANT	BIT 8
131	PITCH OCTANT	BIT 7
132	PITCH OCTANT	BIT 6
133	PITCH DATA	BIT 9
134	PITCH DATA	BIT 8
135	PITCH DATA	BIT 7
136	PITCH DATA	BIT 6
137	PITCH DATA	BIT 5
138	PITCH DATA	BIT 4
139	ALTITUDE	BIT 8
140	ALTITUDE	BIT 7
141	ALTITUDE	BIT 6
142	ALTITUDE	BIT 5
143	ALTITUDE	BIT 4
144	ALTITUDE	BIT 3
145	ALTITUDE	BIT 2
146	ALTITUDE	BIT 1
147	ALTITUDE	BIT 0
148	GAS GAUGING	
149	GAUGING VALID	
150	FUEL CONDITION	
151	ONE ENGINE GAS 1	
152	ONE ENGINE ENG 2	
153	MECHANICAL PRESSURE ENG 1	
154	MECHANICAL PRESSURE ENG 2	
155	MECHANICAL PRESSURE BIT	
156	SPARE 1	
157	SPARE 2	
158	VARIABLE FORMAT DATA	
159	VARIABLE FORMAT DATA	
•	• • •	
•	• • •	
•	• • •	
248	VARIABLE FORMAT DATA	
249	VARIABLE FORMAT DATA	
250	CHECKSUM	BIT 9
251	CHECKSUM	BIT 8
252	CHECKSUM	BIT 7
253	CHECKSUM	BIT 6
254	CHECKSUM	BIT 5
255	CHECKSUM	BIT 4

TABLE 30. RECOMMENDED PRODUCTION AIRS VARIABLE DATA FORMAT

BIT POSITION	DATA	
N	SECONDS	BIT 5
N + 1	SECONDS	BIT 4
N + 2	SECONDS	BIT 3
N + 3	SECONDS	BIT 2
N + 4	SECONDS	BIT 1
N + 5	SECONDS	BIT 0
N + 6	NUMBER TO FOLLOW	BIT 5
N + 7	NUMBER TO FOLLOW	BIT 4
N + 8	NUMBER TO FOLLOW	BIT 3
N + 9	NUMBER TO FOLLOW	BIT 2
N + 10	NUMBER TO FOLLOW	BIT 1
N + 11	NUMBER TO FOLLOW	BIT 0
N + 12	1ST PARAMETER IDENT	BIT 5
N + 13	1ST PARAMETER IDENT	BIT 4
N + 14	1ST PARAMETER IDENT	BIT 3
N + 15	1ST PARAMETER IDENT	BIT 2
N + 16	1ST PARAMETER IDENT	BIT 1
N + 17	1ST PARAMETER IDENT	BIT 0
N + 18	1ST PARAMETER DATA	VSH

ADDITIONAL LINES AS REQUIRED FOR REMAINING DATA

SIGNAL TABLE

PARAMETER	NUMBER OF BITS	DATA BITS	RESOLUTION
AIRSPEED	BITS 10	0 THRU 9	3.04KTS
ENGINE #1 TORQUE	BITS 7	2 THRU 8	2.23 %
ENGINE #2 TORQUE	BITS 7	2 THRU 8	2.23 %
LOADFACTOR	BITS 6	4 THRU 9	0.16 G'S
COLLECTIVE STICK	BITS 5	4 THRU 8	3.2 %
LATERAL STICK	BITS 6	3 THRU 8	1.6 %
LONGITUDINAL STICK	BITS 6	3 THRU 8	1.6 %
PEDAL	BITS 6	3 THRU 8	1.6 %
STABILATOR ACTUATOR #1	BITS 6	4 THRU 9	1.6 %
STABILATOR ACTUATOR #2	BITS 6	4 THRU 9	1.6 %
ALTITUDE RATE	BITS 8	2 THRU 9	40.8 FPM
ICP RATE	BITS 5	3 THRU 7	0.04 GM./CU. METER
ROTOR RPM	BITS 8	4 THRU 11	2% @ 100% RPM
ENGINE #1 RPM (NG)	BITS 6	6 THRU 13	0.36% @ 50% RPM
ENGINE #2 RPM (NG)	BITS 6	6 THRU 13	1.5% @ 100% RPM
HEADING DATA	BITS 8	5 THRU 12	2 DEG.
ROLL DATA	BITS 9	4 THRU 12	1 DEG.
PITCH DATA	BITS 9	4 THRU 12	1 DEG
ALTITUDE	BITS 9	0 THRU 8	100 FEET
SAS WARNING	BITS 1		DISCRETE
SAS/FPS FAULT	BITS 1		DISCRETE
FIRE DETECTION	BITS 1		DISCRETE
CHIP DETECTION ENG 1	BITS 1		DISCRETE
CHIP DETECTION ENG 2	BITS 1		DISCRETE
HYDRAULIC PRESSURE ENG 1	BITS 1		DISCRETE
HYDRAULIC PRESSURE ENG 2	BITS 1		DISCRETE
HYDRAULIC PRESSURE APC	BITS 1		DISCRETE
SPARE 1	BITS 1		DISCRETE
SPARE 2	BITS 1		DISCRETE
VERTICAL G'S	BITS 8	2 THRU 9	2.4 G'S
LATERAL G'S	BITS 8	2 THRU 9	2.4 G'S
LONGITUDINAL G'S	BITS 8	2 THRU 9	2.4 G'S

TABLE 31. RECOMMENDED PRODUCTION AIRS VARIABLE FRAME FORMAT

BIT POSITION	DATA	
0	PROTECT	
1	MINUTES	BIT 7
2	MINUTES	BIT 6
3	MINUTES	BIT 5
4	MINUTES	BIT 4
5	MINUTES	BIT 3
6	MINUTES	BIT 2
7	MINUTES	BIT 1
8	MINUTES	BIT 0
9	FRAME TYPE	1
10	FRAME TYPE	0
11	VARIABLE FORMAT DATA	
12	VARIABLE FORMAT DATA	
13	VARIABLE FORMAT DATA	
14	VARIABLE FORMAT DATA	
15	VARIABLE FORMAT DATA	
16	VARIABLE FORMAT DATA	
17	VARIABLE FORMAT DATA	
18	VARIABLE FORMAT DATA	
19	VARIABLE FORMAT DATA	
20	VARIABLE FORMAT DATA	
.	.	
.	.	
.	.	
228	VARIABLE FORMAT DATA	
229	VARIABLE FORMAT DATA	
230	VARIABLE FORMAT DATA	
231	VARIABLE FORMAT DATA	
232	VARIABLE FORMAT DATA	
233	VARIABLE FORMAT DATA	
234	VARIABLE FORMAT DATA	
235	VARIABLE FORMAT DATA	
236	VARIABLE FORMAT DATA	
237	VARIABLE FORMAT DATA	
238	VARIABLE FORMAT DATA	
239	VARIABLE FORMAT DATA	
240	VARIABLE FORMAT DATA	
241	VARIABLE FORMAT DATA	
242	VARIABLE FORMAT DATA	
243	VARIABLE FORMAT DATA	
244	VARIABLE FORMAT DATA	
245	VARIABLE FORMAT DATA	
246	VARIABLE FORMAT DATA	
247	VARIABLE FORMAT DATA	
248	CHECKSUM	BIT 7
249	CHECKSUM	BIT 6
250	CHECKSUM	BIT 5
251	CHECKSUM	BIT 4
252	CHECKSUM	BIT 3
253	CHECKSUM	BIT 2
254	CHECKSUM	BIT 1
255	CHECKSUM	BIT 0

PARAMETER ASSESSMENT

The data gathered during flight testing has been thoroughly reviewed and analyzed. This evaluation has resulted in some changes to be made which are primarily software in nature.

Altitude currently is read from the transponder associated encoding altimeter. This permits the altitude signal to be turned off in the cockpit. The encoding altimeter is powered by the transponder. When the transponder is off, the AIRS will not receive altitude data. As altitude is a highly important parameter, the signal source should be guaranteed during flight.

The signal source for vertical velocity (altitude rate) was an instrumentation sensor for altitude with a vertical velocity output. This sensor derives vertical velocity directly from the altitude aneroid. The flight test vertical velocity data is extremely erratic. Hamilton Standard does not consider this data representative of this parameter. The production aircraft will use the aircraft's vertical velocity indicator as the signal source. This measures vertical velocity with a pressure vessel that has a "calibrated leak". This should offer excellent damping and reliable accuracy. A resolution of 100 fpm and a floating limit of 200 fpm are recommended for this parameter.

The control positions were all recorded at 3.2% resolution and 6.4% floating limit during initial flight testing. Review of the data obtained indicated that for cyclic position these values resulted in high compression ratios. However, the accuracy of reconstruction was inadequate. The resolution and floating limit were changed to 1.6% and 3.2% respectively on the cyclic and the rudder pedals for further flight testing with excellent results. These are the final recommended values for these parameters.

Heading is currently recorded with 1.8^{o} resolution and floating limit. This results in this parameter having the lowest compression ratio of all parameters. Hamilton Standard recommends increasing the floating limit to 3.6°, as this would improve data compression with minimum impact on data reconstruction.

Review of roll attitude indicates that improvement in data compression could be achieved by using a "dead zone" of about 5 degrees around zero. In other words, do not record any limit exceedance until outside the range of 0 ± 5^{o}. In this way, the normal variations from a nominal steady-state point do not fill up the memory, but data away from that nominal can be recorded accurately.

After engine shutdown and before the AIRS stops recording, the rotor rpm parameter exhibits an anomaly. The design of the frequency interface is such that below 20% rpm the counters underflow and read a high rpm which decreases as the rotor slows further. This results in much erroneous rotor rpm data during the 3 minute period after engine shutdown. This anomaly will be corrected in the system software.

Load factor was flight tested with 0.16g resolution and 0.22g floating limit. Production resolution and limit will be 0.16 and 0.32 respectively. This parameter will also have a dead zone of 1 ± 0.5g. As in roll attitude, this

will filter out normal variations around the nominal steady-state operating point.

The recommendations made in this assessment are in the interest of increasing recording time for a given memory size while preserving or improving the capability to accurately reconstruct the flight data. The recommended parameter list and characteristics are shown in Table 32.

The recommended increases in resolution of the cyclic and rudder pedal position are to provide better data with only an estimated 50% reduction in compression ratio. The resolution changes in vertical velocity, heading, and roll attitude should cause minimum degradation of data reconstruction ability while significantly improving data compression. This is also the reason for imposing an absolute limit or dead band around the nominal values of load factor (1g) and roll attitude (0^{o}). Studies indicate that these changes will effect approximately a 5% increase in data compression and recording time. The reformatting of the data in the memory to reduce the overhead associated with the data has the net effect of increasing the quantity of data that can be stored in the memory although it does not increase the data compression. Studies indicate that this results in a 25 to 40% increase in data capacity. The lesser increase associates with lower activity whereas the higher increase associates with higher activity.

The flight test data when corrected for noisy signals indicates that approximately 10 minutes can be recorded in 32 kilobits of memory and the normal range would be approximately 15 to 45 minutes. With the above recommendations implemented, the minimum time interval stored should be approximately 15 minutes with approximately 22 minutes to an hour being the normal range.

CSMM DESIGN ASSESSMENT

In the past few months, CSMM mechanical improvements have been implemented. In the previous design there was a possibility of water permeating the rubber shell and collecting in the silicone foam around the memory as a result of thermal cycling. There is a probability that sufficient water could collect to cause data errors during dynamic operation and possibly damage the memory during freezing.

The concept shown in Figure 54 is a design modification to correct these conditions. This approach encloses the memory in a hermetically sealed metal package. Internally, the memory is soldered to a two-sided printed circuit board. The I/O signal leads are strain relieved at each solder termination. The interconnected module is potted with a removable material which provides mounting features. The potted module is then enclosed in a hermetically sealed thin-walled metal enclosure which includes a tubular passageway for the interconnect wiring. This hermetically sealed package is then enclosed in the water boiler layers and armored module as in previous CSMM designs. The potted module is protected from direct contact with the water boilers. The raised mounting surfaces of the potted module create an air space within the hermetic enclosure providing room for the water to expand and distribute loading during normal freezing conditions.

TABLE 32. RECOMMENDED PRODUCTION AIRS PARAMETER LIST

PARAMETER	RESOLUTION	FLOATING LIMIT	REMARKS
Airspeed	3.04 k	6.08 k	
Altitude	100 ft	100 ft	Source should not be able to be turned off in cockpit
Vertical Velocity	100 fpm	200 fpm	
Cyclic-Lateral	1.6%	3.2%	
Cyclic-Longitudinal	1.6%	3.2%	
Rudder Pedals	1.6%	3.2%	
Collective	3.2%	6.4%	
Heading	1.8°	3.6°	
Pitch Attitude	0.9°	1.8°	
Roll Attitude	1.8°	3.6°	Absolute Limit 0 ±5°
Rotor RPM	1.9%	3.8%	@ 100% RPM
Engine RPM #1 & #2	1.5% 0.38%	3% 0.76%	@ 100% RPM @ 50% RPM
Engine Torque #1 & #2	2.23%	4.46%	
Load Factor	0.16g	0.32g	Absolute Limit 1 ±0.5g
Impact Acceleration (3-axes)	2.4g		Absolute Limit 0 +7g
Stabilator Position	3.2%	6.4%	Expressed in % of total stroke
Ice Rate	0.04 gm/m^3	0.08 gm/m^3	
SAS/FPS Computer Fault		Any change	Discrete
SAS Warning		Any change	Discrete
Main Fire Detection		Any change	Discrete
Chip Detection #1 & #2		Any change	Discrete
Hydraulic Pressure #1,#2 & APU		Any change	Discrete
Event		Any change	Discrete
Maintenance Readout Unit		Any change	Discrete
Portable Ground Unit		Any change	Discrete
Spares		N/A	Discrete

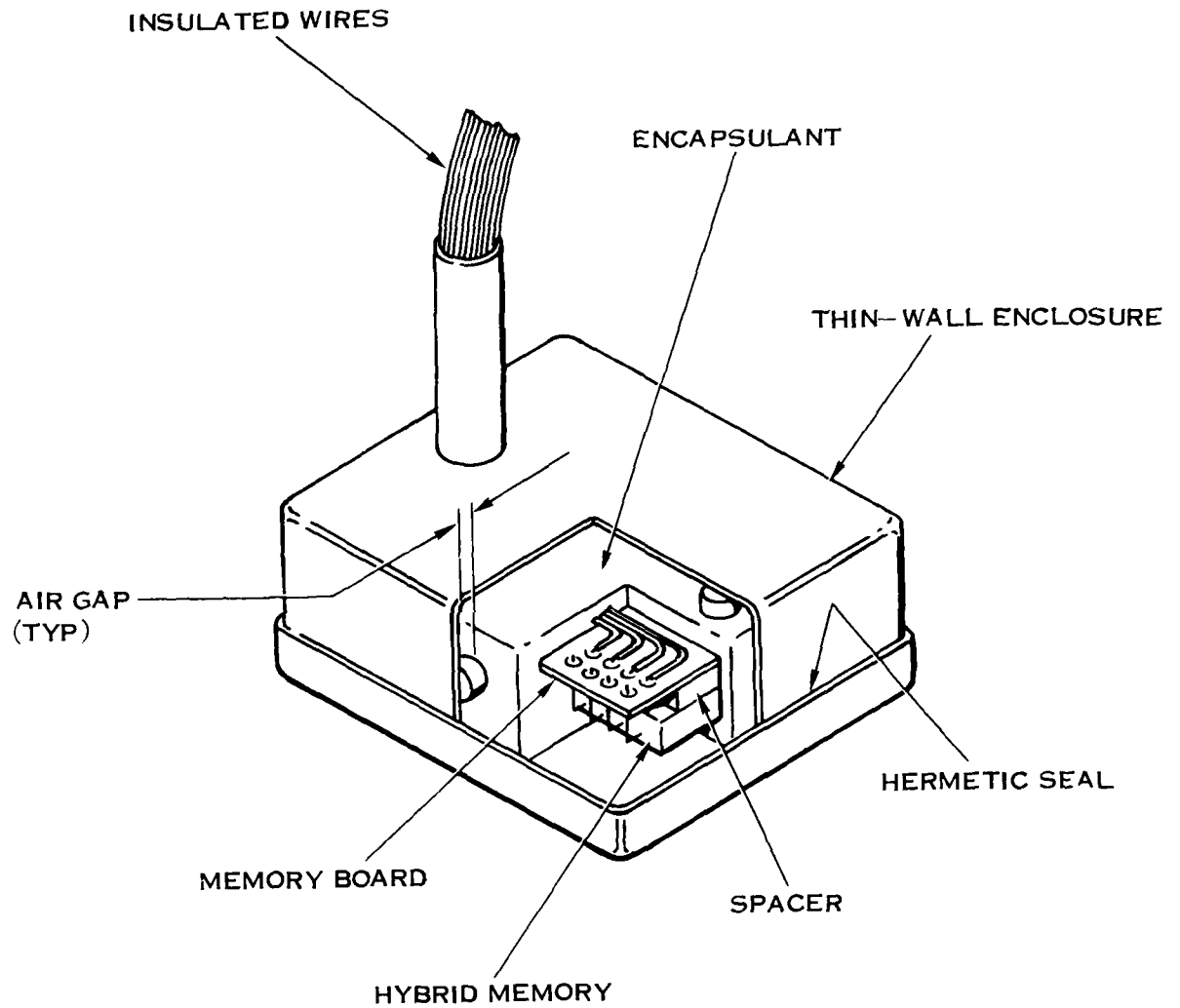


FIGURE 54. HERMETIC MEMORY MODULE

The estimated size, weight, and unit production cost differences between the previous and hermetic concepts are summarized below.

	Previous Concept	Hermetic Concept
Size	4.12 X 3.12 X 2.52 in	3.80 X 3.54 X 2.79 in
Volume	32.4 in^3	37.5 in^3
Weight	3.80 lb	3.80 lb
Unit Production Cost		
Material	100%	93%
Labor	100%	75%

(Memory not included)

Because of the CSMM's small size and because it might be difficult to locate after an aircraft mishap, the possibility of adding a small amount of low level radioactive material is being investigated. The tracer material would assist in the rapid recovery of the CSMM.

Various changes in the mechanical design of the AIRS have been made. Gussets were added to the chassis mounting brackets to ensure meeting the requirement for operation through impacts of up to 150g. The CSMM mounting strap was changed from plastic to aluminum for the same reason. No acceptable plastic material was found that could support the CSMM through a 150g impact.

One connector and two associated flextapes have been added to support an increase in discretes from 24 to 48. The net result of all these changes is an increase in weight of 0.447 pound. The weight of the AIRS is now estimated at 9.23 pounds. There has been no increase in the size estimate of 6.5 X 6.5 X 6.8 inches and the volume of 207 cubic inches.

RISK AREAS DEFINED

The only identified potential risk area uncovered during this program is the possibility of long-term water migration in the CSMM. This phenomenon occurs over very long periods of time. The concern is that the water will permeate the potted module and affect the operation of the memory.

Hamilton Standard feels that the possibility for long-term adverse effects will be minimal with the implementation of the hermetic concept CSMM.

FINAL CONFIGURATION ESTIMATES

Due to various changes in the AIRS electronics unit design, the estimated weight has increased slightly while the size and reliability have remained unchanged. The sensor reliability estimate has increased because a pressure transducer has been deleted from the list. The final configuration estimates are as listed below.

AIRS Electronics Unit

Size: 6.5 inches long X 6.5 inches high X 6.8 inches wide
Weight: 9.23 pounds
Volume: 207 cubic inches
Reliability: 10,300 hours MTBF

AIRS Sensors (4 accelerometers, 2 potentiometers)

Weight: 0.97 pounds
Reliability: 45,450 hours MTBF

AIRS BLACK HAWK Installation

Weight: 5.38 pounds

Total AIRS Flight Data Recorder Installed

Weight: 15.58 pounds
Reliability: 8400 hours MTBF

LIFE-CYCLE COST (LCC) ANALYSIS

This analysis presents the factors used by Hamilton Standard in developing the total efforts associated with the acquisition and ownership of the Accident Information Retrieval System (AIRS) developed under government contract DAAK51-78-C-0025.

The life-cycle cost model is based on USAAVSCOM Technical Report 75-30 (6) entitled "A Computer Model for Aircraft PIP and ECP Economic Analysis". This model is operational on Sikorsky Aircraft's IBM-370 system and is currently used for LCC analysis in support of the BLACK HAWK program and has been approved by Army personnel.

The analysis traces all associated AIRS program costs from Production Design and Development, Production Fabrication and Test, through Operation and Support. In addition, total program costs related to Operation and Support costs have been analyzed through the use of various sensitivity factors listed below:

1. System Mean Time Between Failure (MTBF)
2. System Purchase Cost
3. System Repair Cost
4. Initial Spares
5. Retrofit Kit Purchase Cost
6. Retrofit Kit Depot Installation Cost
7. Production Unit Material Cost
8. Annual Discount Rate Variation
9. Installation Initiation Variation

AIRS PROGRAM PLANS

The time frame for AIRS program initiation was selected as 1 January 1981 for the purposes of this analysis. The program plan covering production Design and Development through Operation and Support was divided into six phases (see Figure 55). As can be noted, the various phases overlap in what is felt to be the most cost effective approach to full utilization and implementation of resources in equipping the BLACK HAWK fleet with the AIRS. The various phases of the program are defined as follows:

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6. USAAVSCOM Technical Report 75-30, A COMPUTER MODEL FOR AIRCRAFT PIP AND ECP ECONOMIC ANALYSIS, August 1975, US Army Aviation Systems Command, Office of the Comptroller, Cost Analysis Division, P.O. Box 209, St. Louis, Missouri 63166.

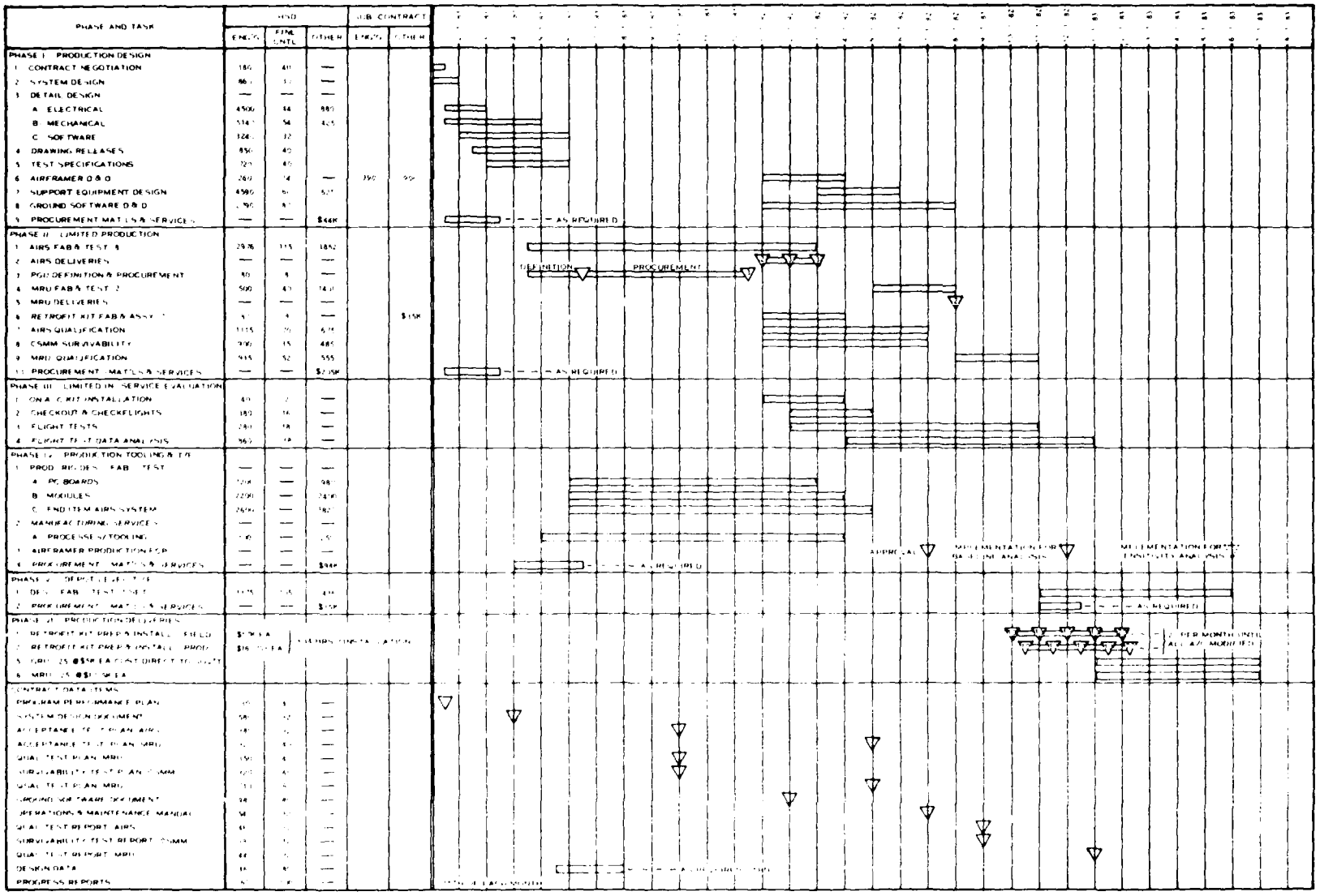

FIGURE 55. AIRS PROGRAM PLAN

Phase I - Production Design

Phase I of the program involves all tasks (and thus all associated nonrecurring costs) necessary to generate detail design drawings, schematics, parts lists, and test specifications required in the fabrication and test of AIRS flight hardware. This hardware definition includes not only the AIRS Electronics Unit and Crash Survivable Memory Module (CSMM) but also the additional aircraft sensors, aircraft wiring, and mechanical installation requirements (ECP generation).

Also included in this phase are the design definitions (drawings, schematics, parts list) for the support hardware to maintain the AIRS at operational capabilities in the field plus software design and development to provide the necessary tools for verifying AIRS generated parametric data on ground-based computer processing facilities.

Phase II - Limited Production

The Limited Production phase of the program involves all the nonrecurring costs associated with the fabrication and test (including qualification and survivability) of production prototype hardware prior to committing to a full scale production program. The limited production of AIRS involves the buildup of eight prototype units for use in qualification testing and limited in service evaluation testing in the field. This phase serves as a pilot program for production planning to ease the transition to high volume production.

The fabrication and test (including qualification) of support hardware is also included in this phase.

Phase III - Limited In-Service Evaluation

This phase involves all nonrecurring costs associated with flight testing and evaluation of information recorded during flight tests using the production prototypes delivered during Phase II of the program. These tests would serve to define any fine tuning required to the production AIRS design prior to committing to high volume production. This phase can also be used to familiarize and train Army personnel in the operation and maintenance of the system hardware and ground software elements.

Phase IV - Production Tooling and Test Equipment

This phase of the program involves all nonrecurring cost associated with the design and development of production rigs and tooling required for the support of a high volume production capability. This includes rigs and fixtures for printed circuit board, module, and end item production acceptance tests. The processes and tooling required to support a high volume production program will also be generated during this phase.

The production schedule shown in Phase VI of the program plan is directly dependent on the completion/prove-out of the Phase IV tasks and thus a direct reason for Hamilton Standard's early initiation of efforts to establish a

fully operational, high volume production capability. The sensitivity analysis related to Installation Initiation Variation covers these cost factors in more detail.

Phase V - Depot Level Test Equipment

This element of the program involves all nonrecurring costs associated with the design, fabrication, test, and delivery of one set of depot level test equipment and user's manuals required in the test and repair of AIRS modules to the piece part level. This cost element is deleted if the Army chooses to return hardware to the manufacturer for repair at the piece part level.

Phase VI - Production Deliveries

The Phase VI element of the program plan involves all recurring costs associated with deliverable AIRS hardware and the operation and support efforts to maintain the deliverable hardware throughout the life of the system. Cost factors involved include:

1. Manufacturing costs related to deliverable AIRS hardware, both electrical and mechanical, procurement of component piece parts, and fabrication.

2. Assembly and test costs involved with production hardware, including quality control, packaging, and transportation through to the contracting agency.

3. Initial spares involving initial provisioning of spare components as necessary for maintenance replacement purposes in end item AIRS and for repair to support newly fielded systems to assure continued operation of the hardware until the pipeline supply system comes into routine operation.

4. Operations costs such as electrical power, computer consumables, operational personnel, and facilities are considered minimal and are not factored into this LCC analysis due to the existence of such requirements now in effect in the Army.

5. Support includes all costs associated with the maintenance of the AIRS and the AIRS support hardware required to maintain the deliverable items in a serviceable condition throughout the life of the hardware. These costs involve procuring activity cost at the line and intermediate level of maintenance and contractor services at the depot level of maintenance.

6. Replenishment spares involve all costs associated with flight hardware spares required to resupply the system stock requirements due to discarding or scrapping of items during the maintenance process.

NOTE: The phase VI effort includes the deliverable ground support hardware (PGU's and MRU's) however, the cost elements associated with this hardware are incorporated as a part of the nonrecurring costs.

NONRECURRING INVESTMENT COSTS

All nonrecurring investment costs, i.e., all costs associated with Phases I through V, support hardware costs, and CDRL item costs depicted in Figure 55, AIRS Program Plan, were based on constant economy (1980). In addition, the costs reflected were based on the development of a high volume production line capability which would allow equipping the total planned Army procurement of 1107 BLACK HAWK helicopters by mid-1991 in line with the production schedule of Sikorsky helicopters. Aircraft previously delivered would be retrofitted by the second month of 1985 assuming retrofit kits are installed in the same month of delivery.

The cost elements presented reflect a single, standard AIRS design applicable to the entire fleet of 1107 aircraft and do not reflect subsequent changes, either through product improvements or procuring activity required modifications/changes, which may subsequently be incorporated entailing added nonrecurring design and development effort and either added or reduced cost factors affecting deliverable system hardware cost and the operation and support cost elements.

The selection rationale of quantities of support hardware required to provide effective data gathering capability from flight hardware and effective maintenance capability over the life of the AIRS included dispersion of aircraft and support equipment functional capabilities and their intended usage.

Portable Ground Unit (PGU)

The PGU is primarily intended to recover data from the AIRS following both major and minor aircraft mishaps. The information retrieved is then made available for expeditious analysis by investigative personnel. The proposed PGU's defined are commercially available, off-the-shelf hardware which can be purchased directly by the procuring activity. The ready availability of the PGU to areas of relatively high aircraft flight activity and to mishap investigation personnel is of prime importance. The quantity suggested takes into account the ready availability of the PGU to mishap investigators at Fort Rucker and at bases where the BLACK HAWK is concentrated. Army personnel have suggested a quantity of 25 for this analysis.

Maintenance Readout Unit (MRU)

The MRU is used at infrequent intervals to assist in the fault isolation of failed AIRS units, including external (to the AIRS) aircraft sensors interfacing to the AIRS when the visual fault indicator on the AIRS unit alerts ground maintenance personnel to a problem. The MRU provides capability of fault isolation of the AIRS to a replaceable module (LRU) level and thus is a useful tool to assist in quickly repairing AIRS at the intermediate level of maintenance.

The quantity suggested would therefore be applicable to major bases where the BLACK HAWK is heavily concentrated. Army personnel have suggested a quantity of 25 for the analysis.

Figure 56 provides a profile of the total nonrecurring investment cost in terms of monthly expenditures as a percentage of the total. The investment profile presents the monthly nonrecurring cost factors related to the proposed plan phases in Figure 55.

RECURRING COSTS

The recurring cost elements of the analysis include the total quantity of AIRS required to equip the entire fleet of Army planned BLACK HAWK procurement of 1107 aircraft, the initial spares required to sustain the newly purchased system operational capabilities, and the replenishment spares required to maintain the flight hardware over the full life of the system. The life cycle of the system for this analysis is 20 years.

The factors involved with each category of recurring costs defined above are as follows:

Original Hardware Procurement and Installation

Original hardware procurement is determined by the total number of aircraft planned for the fleet less the number of attrited aircraft expected during the AIRS procurement and installation cycle using an aircraft attrition factor of 16 per one million fleet flying hours. Fleet flight hours are determined using a factor of 25 flight hours per aircraft per month for the entire fleet which is in operation at the start of the analysis and those aircraft which are scheduled to become operational during the AIRS procurement cycle. Fleet flight hours accumulated prior to 1 January 1981 are disregarded in the analysis.

The cost elements involved in kit hardware and installation included one AIRS Electronics Unit with attached Crash Survivable Memory Module (CSMM), four accelerometers including three for measuring the three axes of impact acceleration and one for the normal load factor, two potentiometric devices for measuring pedal position and lateral stick position (since these are not presently installed on production BLACK HAWK aircraft), and the wiring and bracketry necessary to incorporate the above in the production aircraft.

Labor for kit manufacture and preparation and kit installation (for both production installation and field retrofit) complete the cost elements involved in original hardware procurement and installation.

The delta effect on recurring costs for this cost element was analyzed by varying the factors below over a range of values:

1. New Item Purchase Cost

   Original estimate of spares kit cost increased by 36% in 3% increments.

2. Retrofit Kit Purchase Cost

   Original estimate of retrofit kit was varied over a range of -12% to +21% in 3% increments.

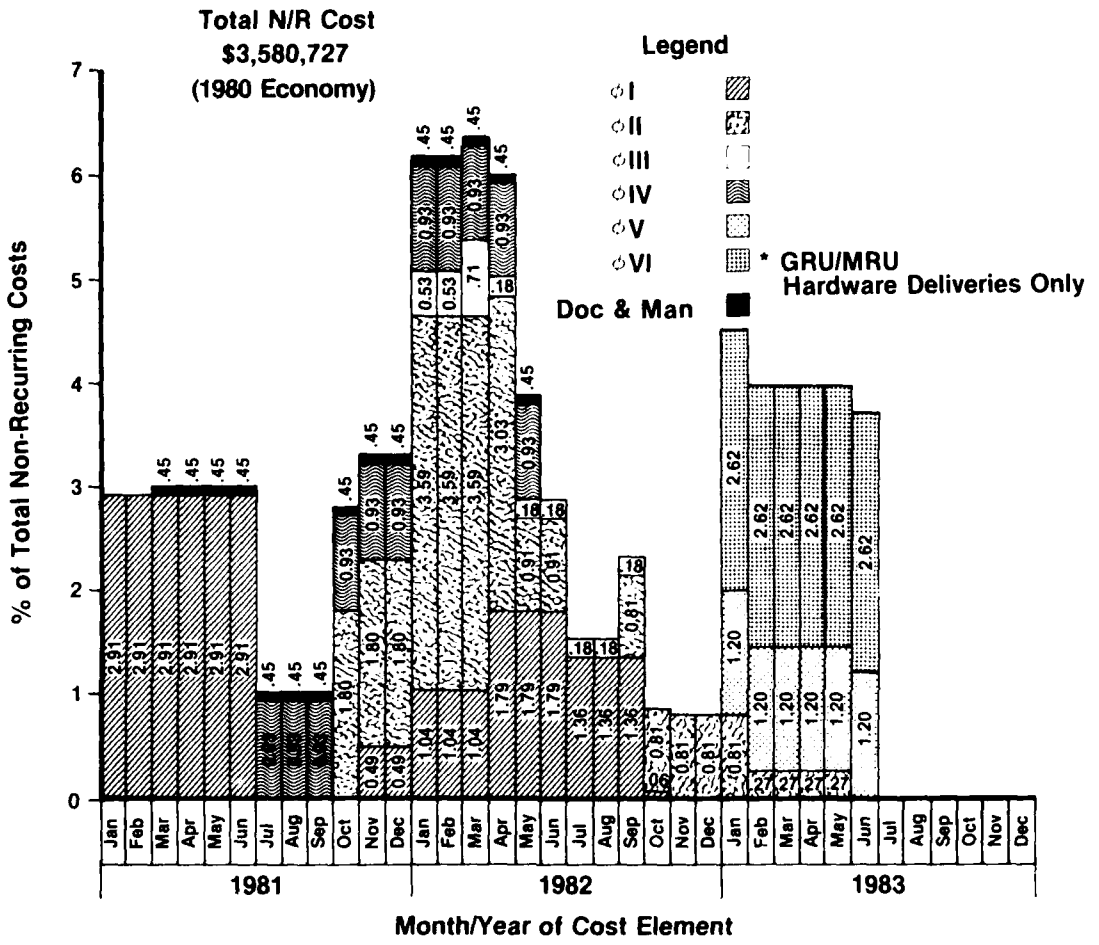

FIGURE 56. AIRS NONRECURRING PROGRAM COST SUMMARY

Initial Spares

The initial spares cost element selected for the analysis was 5%. This factor allows filling of the pipeline to sustain the newly installed hardware in an operational readiness condition until such time that replenishment spares for failed items become available and/or failed items are repaired.

Initial spares cost includes all hardware and associated preparation labor as defined for the retrofit kits described in the original hardware procurement cost element.

Replenishment Spares

This cost element deals with the repair or replacement of failed items at both the intermediate and depot levels of maintenance. This cost factor occurs only when a part of the AIRS fails. The failure rate specified for the AIRS is 7700 hours (MTBF). A sensitivity factor of -28% MTBF to +50% MTBF in increments of 500 hours was used in the analysis to determine the effects of either improving or degrading MTBF.

Costs at the intermediate level of maintenance utilized factors for repair and replacement as defined below:

1. Man-hours to replace a failed item in the field or depot of 1.0 including test setup, fault isolation, replacement of failed module, and verification of repair.

2. Depot repair to the component level. It is the recommendation that the depot level repair be performed by the manufacturer, as this would be the most economical approach. Total cost involved over the life of the system involving repair of failed items to the component level is only slightly higher than the cost involved in the purchase of Depot Level Test Equipment which is already available at the manufacturer's facility. A repair factor of 3.62 hours per failure and nominally $500 in materials was determined for the AIRS based on a similar system already in operation on the BLACK HAWK (i.e., the flight control computer). A scrap factor of 6% for the AIRS was also utilized in the determination of repair costs which would amount to approximately ten systems over the life of the hardware.

The graph shown in Figure 57 depicts all recurring cost elements in discounted (at a 10% rate) dollar percentages of the LCC analysis on a per-year basis as a percentage of the total recurring flyaway costs with the various cost elements identified.

Figure 58 summarizes all costs associated with the AIRS Program Plan, including both nonrecurring and recurring, in discounted (at a 10% rate) dollar percentages.

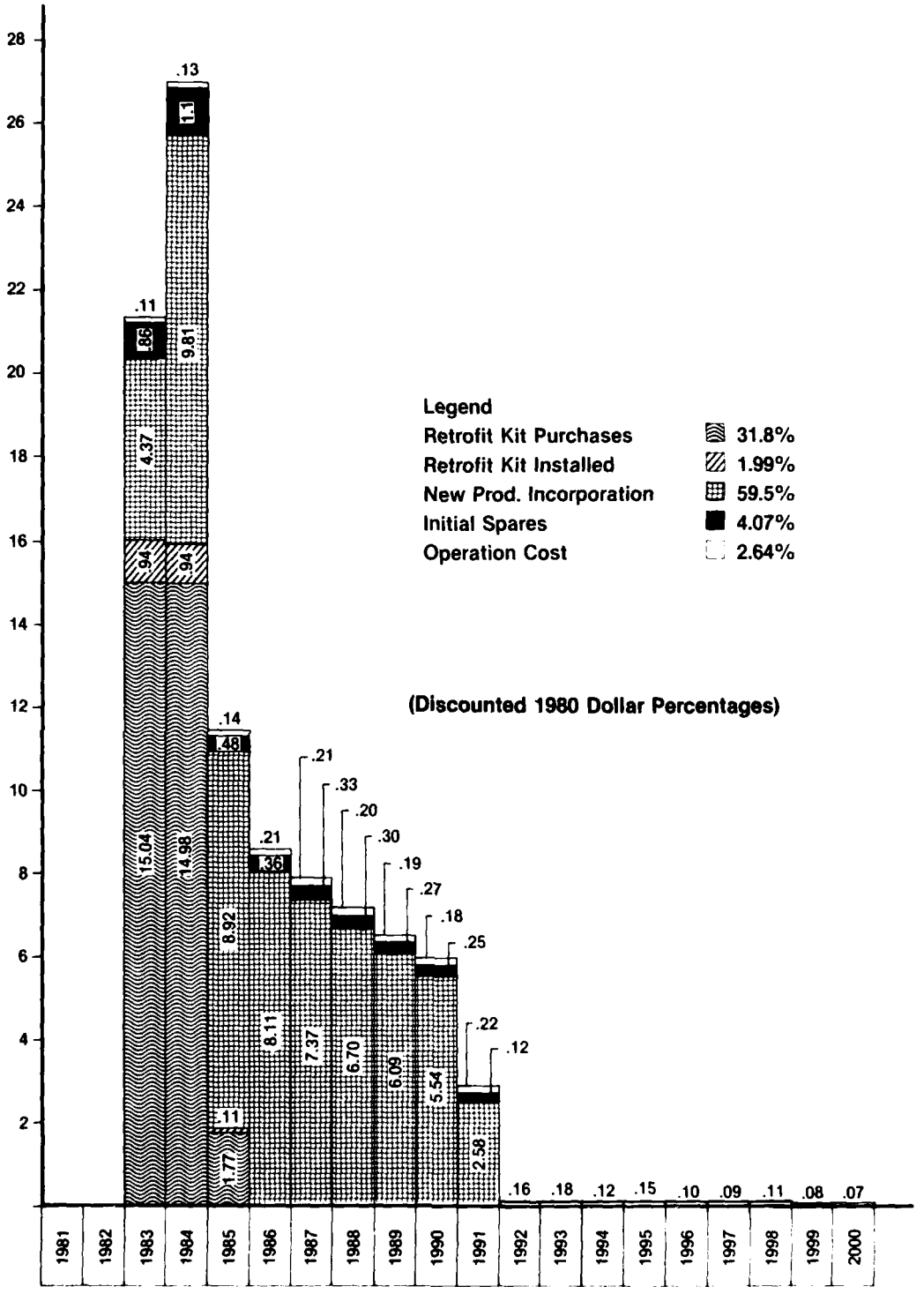

FIGURE 57. AIRS TOTAL PROGRAM RECURRING COSTS

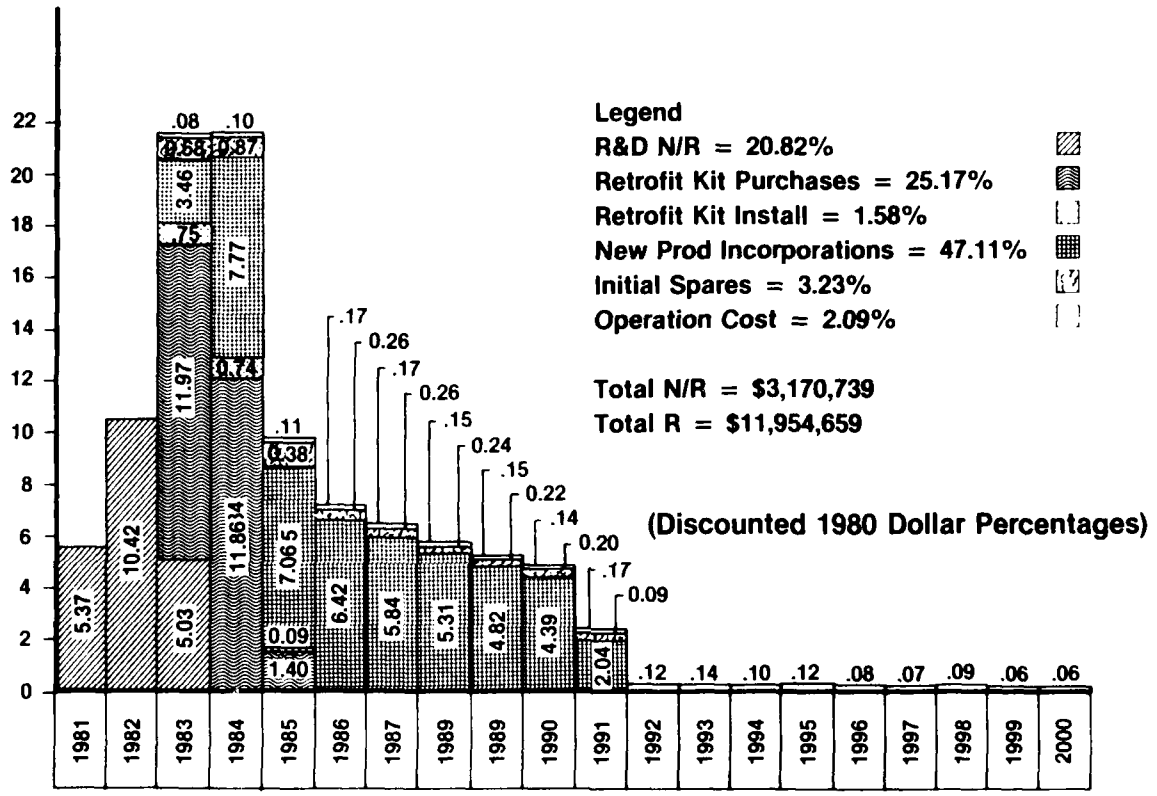

FIGURE 58. AIRS TOTAL PROGRAM COSTS

CONCLUSIONS

The conclusions derived from the AIRS detailed design, fabrication, and test program are as follows:

1. The technology for a low cost, lightweight, solid-state flight data recorder suitable for application in small tactical rotary wing aircraft in the Army inventory is available.

2. The AIRS can accommodate a significant complement of aircraft parametric data including DC and AC analogs, frequencies, and discretes while providing storage capabilities sufficient to record, recover, and eventually recreate the critical flight regime leading to an aircraft major or minor incident/accident.

3. Data compression techniques developed for AIRS can allow a significant amount of data storage without compromising the integrity of aircraft parametric information.

4. The high reliability inherent in the AIRS solid-state design insures minimization of operational support and maintenance costs.

5. With the availability of higher order memory storage devices, the AIRS can be economically expanded to handle significantly more aircraft parameters and store significantly more data at relatively small increases in cost and size. This expansion capability would thus allow use of the basic AIRS concept in a variety of aircraft types. Additionally, the use of the AIRS in maintenance functions related to engine condition monitoring, structural integrity monitoring, and aircraft performance monitoring could also be realized.

RECOMMENDATIONS

The recommendations are as follows:

1. Proceed into production design of the AIRS based on system design criteria that have been developed and demonstrated through environmental and flight test.

2. Undertake further study on the life-cycle cost benefits of a single hardware design for a class of Army rotary and fixed wing aircraft prior to or in parallel with a production design effort.

REFERENCES

1. H.Ask, et al, PRELIMINARY DESIGN OF AN ACCIDENT INFORMATION RETRIEVAL SYSTEM (AIRS), USARTL 77-51, Applied Technology Laboratory, U.S. Army Research and Technology Laboratories (AVRADCOM), Fort Eustis, Virginia, April 1978, AD055590.

2. U.S. Federal Aviation Regulation, Part 37.150, AIRCRAFT FLIGHT RECORDER TECHNICAL STANDING ORDER, TSO-C51a.

3. NADC 78170-50, BUBBLE MEMORY DEVICE CHARACTERIZATION STUDY, November 1979, Rockwell International, Autonetics Strategic Systems Division, P.O. Box 4192, 3370 Miraloma Ave., Anaheim, California 92803.

4. NADC 78175-50, BUBBLE MEMORY DEVICE CHARACTERIZTION STUDY, February 1980, Texas Instruments Inc., Central Research Lab., 13500 North Central Expressway, Dallas, Texas 75265.

5. Sikorsky Engineering Report, SER70078 - UTTAS FLIGHT TEST VEHICLE NOS. 1, 2 AND 3 - AIRBORNE DATA ACQUISITION SYSTEM, Prepared under Contract DAAO01-73-C-0006 (PGA), P00100, 17 November 1978, Sikorsky Aircraft, Stratford, Connecticut.

6. USAAVSCOM Technical Report 75-30, A COMPUTER MODEL FOR AIRCRAFT PIP AND ECP ECONOMIC ANALYSIS, August 1975, U.S Army Aviation Systems Command, Office of the Comptroller, Cost Analysis Division, P.O. Box 209, St. Louis, Missouri 63166.

ABBREVIATIONS AND SYMBOLS

A	Angstrom - unit measurement of wavelength
AAH	Advanced attack helicopter
AC	Alternating current
A/D	Analog to digital
AIRS	Accident information retrieval system
APU	Auxiliary power unit
ARINC	Aeronautical Radio Incorporated
BAUD	A digital word rate in coded samples per second
BCD	Binary coded decimal
BIT	Built-in-test
BORAM	Block Oriented Random Access Memory
BOT	Beginning of tape
BYTE	A subset of bits in a larger digital word structure
CCD	Charge coupled device
CMOS	Complimentary metal oxide semiconductor
CPU	Central processing unit
CRC	Cyclic redundancy check
CDRL	Contract data requirements list
CRT	Cathode ray tube type of computer terminal
CSMM	Crash survivable memory module
CVR	Cockpit voice recorder
D/A	Digital to analog
DC	Direct current

DEG(°)	Degrees
DEO	Development engineering order
DFDR	Digital flight data recorder
DIP	Dual inline package
EAROM	Electrically alterable read only memory
E^2 PROM	Electrically erasable programmable read only memory
EGT	Exhaust gas temperature
EMI	Electromagnetic interference
EOT	End of tape
EWR	Engineering work request
FAA	Federal Aviation Administration
FAR	Federal Aviation Regulation
FIFO	First in first out memory
FPM	Feet per minute
FT	Feet
F.S.	Full scale
G(g)	Acceleratioin of gravity
GI	General Instruments
gm/m^3	Grams per cubic meter
IC	Integrated circuit
ID	Identification
IN	Inch(es)
H	Hexadecimal
Hz	Hertz
I^2L or IIL	Integrated injection logic

I/O	Input/output
K	Thousand
KHz	Kilohertz
k	Nautical miles per hour (knots)
LAMBDA (λ)	Failure Rate - Per 1,000,000 units, Operating
LB	Pound(s)
LED	Light emitting diode
LSB	Least significant bit
LSI	Large scale integration
LSTTL	Low power schottky transistor transistor logic
MHz	Megahertz
MIB	Master interconnect board
MMH	Maintenance man-hour
MNOS	Metal nitride oxide semiconductor
MOS	Metal oxide semiconductor
MRU	Maintenance readout unit
MSB	Most significant bit
MTBF	Mean time between failures
MTBUR	Mean time between unscheduled removals
MTTR	Mean time to repair
MUX	Multiplexer
mV	Millivolt
mS or msec	Millisecond
μS	Microsecond

N/A	Not applicable
NCR	National Cash Register
N_G	Engine rotational speed
NMOS	N channel metal oxide semiconductor
N_R	Rotor rotational speed
%	Percent of 100
PC	Printed circuit
PCM	Pulse code modulation
PGU	Portable ground unit
PLA	Power lever angle
PMOS	P Channel metal oxide semiconductor
PSID	Pounds per square inch differential
PTT	Press to talk
PWM	Pulse width modulator
QAR	Digital flight data quick access recorder
RAM	Random access memory
RAPID	Real time acquisition and processing of inflight data
ROM	Read only memory
RPM	Revolutions per minute
RS232	Electronics Industries Association data interface standard
RSS	Root sum squared
SAS/FPS	Stability augmentation system/flight path stabilization
SEC	Second(s)
TSO	Technical standing order
T^2L or TTL	Transistor transistor logic

VAC	Volts - alternating current
VDC	Volts - direct current
VPP	Volts - peak to peak
VRMS	Volts - root mean square
WW	Wire wrap
<	Greater than
>	Less than
| XY |	Absolute value of product of number values represented by X and Y